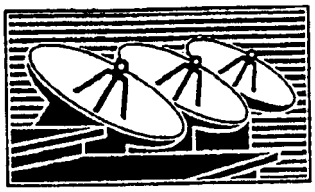

530—STGT—IE310

OPERATION AND MAINTENANCE MANUAL

MODULATOR/DOPPLER PREDICTOR

April 1992

National Aeronautics and Space Administration

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

OPERATION AND MAINTENANCE MANUAL

MODULATOR/DOPPLER PREDICTOR

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Change Information Page

List of Effective Pages			
Page Number	**Issue**	**Page Number**	**Issue**
Title	Original	4–9	DCN–003
iii	DCN–003	4–10	DCN–001
iv through viii	DCN–001	4–11 through 4–15	Original
ix	DCN–002	4–16	DCN–002
x through xii	DCN–001	4–17 and 4–18	Original
1–1 and 1–2	DCN–001	4–19	DCN–001
1–3	Original	4–20	Original
1–4 and 1–5	DCN–001	4–21 and 4–22	DCN–001
1–6	Original	4–23 and 4–24	Original
1–7	DCN–001	5–1 and 5–2	DCN–001
1–8	DCN–002	5–3 through 5–5	Original
1–9	DCN–001	5–6	DCN–001
1–10 through 1–18	Original	5–7 through 5–16	Original
2–1 through 2–6	Original	6–1 and 6–2	Original
3–1 through 3–3	Original	6–3 through 6–5	DCN–001
3–4	DCN–001	6–6 through 6–12	Original
3–5 through 3–10	Original	7–1 and 7–2	Original
3–11	DCN–001	G–1 and G–2	Original
3–12 through 3–14	Original		
3–15	DCN–001		
3–16	Original		
4–1	Original		
4–2 and 4–3	DCN–001		
4–4	Original		
4–5	DCN–001		
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DCN CONTROL SHEET

Use this control sheet to record the DCN changes to this document.

DCN	DTG	Mon/Yr	Sect.	Initials

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TABLE OF CONTENTS

Paragraph	Title	Page
	Section 1 — General Description	
1−1	Introduction	1−1
1−2	Physical Description	1−3
1−3	Functional Description	1−5
1−3.1	MDP Chassis Assembly	1−5
1−3.2	Power Supply No. 1	1−6
1−3.3	Power Supply No. 2	1−6
1−3.4	Modem Control Processor PWA	1−6
1−3.4.1	MCP Functions	1−6
1−3.4.2	MCP Interfaces	1−7
1−3.5	Data Conditioning And Encoding PWA	1−7
1−3.5.1	DCEC Functions	1−7
1−3.5.2	DCEC Interfaces	1−8
1−3.6	Timing Generator PWA	1−8
1−3.6.1	TIME Functions	1−8
1−3.6.2	TIME Interfaces	1−8
1−3.7	Synthesizer PWA	1−8
1−3.7.1	SYNTH Functions	1−8
1−3.7.2	SYNTH Interfaces	1−9
1−3.8	Forward Modulator PWA	1−9
1−3.8.1	FMOD Functions	1−9
1−3.8.2	FMOD Interfaces	1−9
1−3.9	Ground Network Modulator PWA	1−9
1−4	Condensed Data	1−9
1−5	Special Tools and Test Equipment	1−18
	Section 2 — Installation	
2−1	Introduction	2−1
2−2	Chassis Installation In STGT	2−1
2−3	Unpacking	2−1
2−4	Chassis Installation	2−1
2−5	Chassis Removal	2−4
2−6	Unit Packaging	2−4
2−7	PWA Packaging	2−5
2−8	Storage	2−6
2−8.1	Short−Term Storage	2−6
2−8.2	Long−Term Storage	2−6
2−9	Shipment	2−6

Paragraph	Title	Page
	Section 3 — Operation	
3−1	Introduction	3−1
3−2	Modes Of Operation	3−1
3−3	Remote Control	3−1
3−4	Local Control	3−1
3−5	Safety	3−1
3−6	Equipment Access	3−2
3−7	Controls And Indicators	3−2
3−8	Self−Check	3−2
3−9	Turn−On	3−2
3−10	Built−In Test	3−2
3−11	Normal Operation	3−7
3−12	Emergency Operation	3−9
3−13	Shutdown	3−9
3−14	BIT Features	3−9
3−15	Confidence Bit	3−9
3−15.1	RAM Test	3−13
3−15.2	CPU Test	3−13
3−15.3	Kernel Initialization	3−14
3−15.4	Interrupt Initialization	3−14
3−15.5	MIL−STD−1553 Test	3−14
3−15.6	I/O Initialization	3−14
3−15.7	VME Test	3−14
3−15.8	Environment Test	3−14
3−15.9	Indicators Test	3−14
3−16	Online Bit	3−14
3−16.1	Monitor Exceptions	3−15
3−16.2	Monitor Time	3−15
3−16.3	Monitor Environment	3−15
3−16.4	Monitor Synthesizer Lock	3−15
3−16.5	Monitor 1 PPS	3−15
3−16.6	Monitor ALC Levels	3−15
3−17	Extended Bit	3−15
3−17.1	MCP Test	3−16
3−17.2	VME Test	3−16
3−17.3	TIME Test	3−16
3−17.4	DCEC Test	3−16
	Section 4 — Theory of Operation	
4−1	Introduction	4−1
4−2	Detailed Functional Description	4−1
4−3	Firmware Descriptions	4−1
4−3.1	Executive Program	4−1

Paragraph	Title	Page
4—3.2	MDP Program	4—3
4—4	States Of Operation	4—5
4—5	MDP Configurations	4—5
4—6	Carrier/Code Compensation	4—5
4—7	Carrier Sweep and Break Lock	4—9
4—8	Command and Range PN Channels	4—9
4—9	Data Input Processing	4—10
4—9.1	SSA Forward Service (SSAF)	4—10
4—9.2	SSH Forward Service (SSHF)	4—10
4—9.3	KSA Forward Service (KSAF)	4—10
4—9.4	KSH Forward Service (KSHF)	4—10
4—9.5	MA Forward Service (MAF)	4—10
4—10	Modem Control Processor PWA	4—11
4—10.1	68030 Microprocessor	4—11
4—10.2	EPROM and SRAM	4—11
4—10.3	Serial I/O Interfaces	4—11
4—10.4	MPCC Interrupt Handling	4—11
4—10.5	VMEbus Interface	4—13
4—10.6	MCP Function Switches And LEDS	4—13
4—10.7	BERR Handling	4—14
4—11	Data Conditioning and Encoding PWA	4—14
4—11.1	Data Format Conversion	4—14
4—11.2	Convolutional Encoding	4—14
4—11.3	Phased—Lock Loop	4—14
4—11.4	Symbol Format Conversion	4—14
4—11.5	PN Spreading	4—14
4—11.6	Clock Detection	4—16
4—11.7	Data Presence Detection	4—16
4—11.8	DCEC Registers	4—16
4—12	Timing Generator PWA	4—16
4—12.1	IRIG Decoding	4—16
4—12.2	1553 Interface	4—16
4—12.3	Time Mark Generation	4—18
4—12.4	Interrupt Generation	4—18
4—12.5	Epoch Count Generation	4—18
4—12.6	NCO Outputs	4—18
4—12.7	Analog—To—Digital Generation	4—18
4—12.8	Miscellaneous Registers and Control	4—18
4—12.9	RF Status and Control	4—19
4—13	Synthesizer PWA	4—19
4—14	Forward Modulator	4—19
4—14.1	70—MHz UQPSK Modulator	4—19
4—14.2	Modulated 370—MHz IF Output (Low Data Rate Mode)	4—22
4—14.3	Modulated 370—MHz IF Output (High Data Rate Mode)	4—22

Paragraph	Title	Page
4−14.4	Unmodulated 370−MHz IF Output	4−22
4−14.5	Automatic Level Control	4−22
4−15	GN Modulator PWA	4−22
4−16	Modulator/Doppler Predictor External Interface Description	4−22
4−17	Modulator/Doppler Predictor Internal Interface Description	4−22
4−18	Mechanical Components	4−22
	Section 5 — Maintenance	
5−1	Introduction	5−1
5−2	Performance Standards	5−2
5−3	Test And Adjustment Procedures	5−2
5−4	Fault Isolation (Troubleshooting)	5−4
5−5	Preliminary Fault Isolation Steps	5−7
5−6	Operational Verification	5−7
5−7	Removal/Replacement	5−8
5−8	PWA Replacement	5−9
5−9	IC Chip Replacement	5−9
5−10	Cooling Fan Replacement	5−12
5−11	PS1 and PS2 Replacement	5−13
5−12	Lamp Replacement	5−13
5−13	Lampholder Replacement	5−14
5−14	Switches and Circuit Breaker Replacement	5−15
5−15	Preventive Maintenance	5−15
5−16	Inspection	5−16
5−17	Preventive Maintenance Steps	5−16
	Section 6 — Parts List	
6−1	Introduction	6−1
6−2	List of Manufacturers	6−1
6−3	Maintenance Parts List	6−1
6−4	Reference Designator Column	6−1
6−5	Figure and Index Number Column	6−1
6−6	Description Column	6−1
6−7	CAGE/FSCM Column	6−1
6−8	Part Number Column	6−1
6−9	Quantity Column	6−1
6−10	Illustrations	6−2
	Section 7 — Drawings	
7−1	Introduction	7−1
	Glossary	
	Glossary	G−1

LIST OF ILLUSTRATIONS

Figure	Title	Page
	Section 1 — General Description	
1−1	Modulator/Doppler Predictor P/N 7472300	1−4
1−2	Modulator/Doppler Predictor Interfaces for the MA Receiver/Transmit and SSA Equipment Configurations	1−6
1−3	Modulator/Doppler Predictor Interfaces for the KSA Low Data Rate Equipment Configuration	1−7
	Section 2 — Installation	
2−1	Modulator/Doppler Predictor Rear Panel	2−2
2−2	Equipment Packing/Unpacking	2−3
	Section 3 — Operation	
3−1	Modulator/Doppler Predictor Front and Maintenance Panel	3−3
3−2	Modulator/Doppler Predictor PWA Front Panels	3−4
3−3	Power Supply No. 1 Control and Indicators	3−5
3−4	Power Supply No. 2 Controls	3−5
	Section 4 — Theory of Operation	
4−1	Modulator/Doppler Predictor Functional Block Diagram	4−2
4−2	MDP Operating States	4−6
4−3	Modulation Configuration Used for Non−Shuttle MA, SSA, and KSA Bit Rates Less Than or Equal to 300 Kbps	4−7
4−4	Modulation Configuration Used for Shuttle K−Band and KSA Bit Rates Greater Than 300 Kbps	4−7
4−5	Modulation Configuration Used for Shuttle S−Band	4−8
4−5−a	Modulation Configuration Used for Subcarrier and Direct Phase Modulation	4−8
4−6	MCP Functional Block Diagram	4−12
4−7	DCEC Functional Block Diagram	4−15
4−8	TIME Functional Block Diagram	4−17
4−9	SYNTH Functional Block Diagram	4−20
4−10	FMOD Functional Block Diagram	4−21
	Section 5 — Maintenance	
5−1	Power Supply No. 1 Voltage Adjustments	5−3
5−2	Power Supply No. 2 Voltage Adjustments	5−4
5−3	MCP PWA Component Location Diagram	5−10
	Section 6 — Parts List	
6−1	Modulator/Doppler Predictor (Top View)	6−4
6−2	Modulator/Doppler Predictor (Front View)	6−6
6−3	Modulator/Doppler Predictor (Side View)	6−8
6−4	Modulator/Doppler Predictor (Rear View)	6−10

LIST OF TABLES

Table	Title	Page
	Section 1 — General Description	
1−1	MDP Commands and Reports	1−2
1−2	Major Components	1−5
1−3	Electrical Characteristics	1−10
1−4	NASA Drawings	1−16
1−5	Environmental Requirements	1−17
1−6	Equipment Required, but Not Supplied	1−17
1−7	Consumables	1−17
1−8	Special Tools and Test Equipment	1−18
	Section 3 — Operation	
3−1	Modulator/Doppler Predictor Front Panel Controls and Indicators	3−6
3−2	Modulator/Doppler Predictor Maintenance Panel Controls and Indicators	3−8
3−3	Modulator/Doppler Predictor PWA Controls and Indicators	3−10
3−4	Power Supply No. 1 Controls and Indicators	3−12
3−5	Power Supply No. 2 Controls	3−13
	Section 4 — Theory of Operation	
4−1	PN Configurations	4−4
4−2	MDP Carrier Tuning Ranges	4−8−a
4−3	External Interface Signal	4−23
	Section 5 — Maintenance	
5−1	Replaceable LRUs	5−1
5−2	Modulator/Doppler Predictor Maintenance Concept	5−2
5−3	Fault Isolation	5−5
5−4	MCP Jumper Configurations	5−11
5−5	Inspection and Maintenance Criteria	5−16
	Section 6 — Parts List	
6−1	List of Parts Lists and Figures	6−2
6−2	Index to Manufacturers CAGE/FSCM Numbers	6−3
6−3	Parts List, Modulator/Doppler Predictor (Top View)	6−5
6−4	Parts List, Modulator/Doppler Predictor (Front View)	6−7
6−5	Parts List, Modulator/Doppler Predictor (Side View)	6−9
6−6	Parts List, Modulator/Doppler Predictor (Rear View)	6−11
	Section 7 — Drawings	
7−1	List of Drawings	7−1

Section 1 — General Description

1−1 Introduction

1−1.1 This Level 1 manual is limited to unit operation and maintenance in the installed condition while in local (maintenance) control. Also included is the information necessary to replace and maintain the chassis and all applicable line replaceable units (LRUs) for the Modulator/Doppler Predictor (MDP), part number 7472300.

1−1.2 The MDP provides forward modulation, carrier and code Doppler compensation, and carrier sweep for all S−Band Single Access (SSA), K−Band Single Access (KSA), and Multiple Access (MA) forward user services.

1−1.3 The MDP provides the following essential functions, as required, when applicable:

a. Provide data formatting, symbol formatting, and encoding of forward user data.

b. Provide data presence monitoring.

c. Generate PN codes and clocks.

d. PSK modulate the forward carrier with forward data and PN codes, or PM modulate the forward carrier with PCM−formatted forward data or with a BPSK subcarrier modulated by the PCM−formatted forward data. Output modulation will be at a nominal 370 MHz IF.

e. Provide forward link Doppler compensation, including the capability to:

   (1) Simultaneously adjust the forward link carrier frequency and PN code rate in accordance with a commanded profile.

   (2) For S−Shuttle support, independently Doppler compensate the carrier and PN code rate.

   (3) Receive Doppler updates from the data bus via the primary interface.

   (4) Enable and disable Doppler compensation as commanded.

f. Assist user satellite (USAT) acquisition or reacquisition, provide the capability to sweep the forward carrier and PN code, or, to force a reacquisition, provide a step in carrier and code frequency to break lock on the forward link.

g. Provide tuning of the carrier frequency to accommodate service assignment (SSA, KSA, and MA) and user frequency assignment.

h. Provide support for tracking services including:

   (1) Time transfer measurement.

   (2) Range zero set.

i. Generate status data, including self−test and fault isolation information.

j. Generate test signals, including an unmodulated IF carrier output.

k. Communicate with the primary interface via the MIL−STD−1553B data bus. Table 1−1 lists the various commands and report names and fields used to communicate over the 1553 bus.

l. Support maintenance and operation, provide front panel and maintenance panel controls, indicators, and test points, as specified.

1−1.4 The information in this manual is presented in seven sections: Section 1, General Description; Section 2, Installation; Section 3, Operation; Section 4, Theory of Operation; Section 5, Maintenance; Section 6, Parts list; and Section 7, Drawings.

1−1.5 Section 1 describes the use, capabilities, and technical specifications of the MDP. The MDP (see figure 1−1; shown with top cover removed) is an integral part of the Second Tracking and Data Relay Satellite System (TDRSS) Ground Terminal (STGT) Forward User Services Subsystem (USS).

1−1.6 This OP−06−1 manual was prepared for the National Aeronautics and Space Administration (NASA) by GE Contract No. NAS5−33000.

Table 1—1. MDP Commands and Reports

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
SET STATE	Start checkword Initialization type Initialization data End checkword	CONFIGURATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Service type Feedback taps Register A initialization condition Operational light Shuttle mode SSHF PN compensation rate Forward data rate Modulation type Modulation index for GN modes Subcarrier frequency Subcarrier—to—data rate ratio GN data format Idle pattern enable Modulation enable/disable End checkword
SPECIFIC CONFIGURATION	Start checkword Configuration item bit map Service type Shuttle mode Feedback taps Register A initialization condition Operational light SSHF PH code rate Forward data rate Modulation type Modulation index for GN modes Subcarrier frequency Subcarrier—to—data rate ratio GN data format Idle pattern enable Modulation enable/disable End checkword		
COMMON CONFIGURATION	Start checkword Bit map Forward IF offset frequency Forward translation frequency Modulation configuration Doppler compensation configuration SN/GN forward sweep select GN forward sweep duration GN forward sweep range End checkword	COMMON CONFIGURATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds PN modulation configuration Doppler compensation configuration SN/GN forward sweep select GN forward sweep duration GN forward sweep range End checkword
DOWNLOAD	Start checkword Download type 1553 word count End checkword	TIME TRANSFER	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds 1st epoch measurement End checkword
FORWARD FREQUENCY SWEEP	Start checkword Effective time; hours Effective time; minutes Effective time; seconds End checkword	PERFORMANCE	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Lock status Commands not executed map
FORWARD DOPPLER CONTROL	Start checkword Effective time; hours Effective time; minutes Effective time; seconds Command word Duration		

Table 1−1. MDP Commands and Reports (Continued)

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
FORWARD DOPPLER CONTROL (Continued)	Delta target frequency Return to profile End checkword	PERFORMANCE (Continued)	Commands not accepted map Commands not executed error code Commands not accepted error code Operating state Delta IF frequency Ephemeris status Frequency control status Input data presence PN code state Confidence test Online BIT status Local/remote status End checkword
START SERVICE	Start checkword Effective time; hours Effective time; minutes Effective time; seconds End checkword		
FORWARD BREAK LOCK	Start checkword Effective time; hours Effective time; minutes Effective time; seconds Duration Step size End checkword		
		EXTENDED BIT	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds MCP test results VME test results TIME test results DCEC test results End checkword
EPHEMERIS DATA	Start checkword Time of first point; hours Time of first point; minutes Time of first point; seconds Number of points per table Table select bit map Doppler compensation table Doppler pre−correction table Delay table TDRS Doppler table End checkword		

1−2 Physical Description

For the purposes of this manual, the major components described are those that are maintained, replaced, or repaired in the installed condition (Level 1 LRUs). Refer to table 1−2 for a listing of the major components (LRUs) of the MDP and the illustrations in section 6 for their location. The following information describes the physical characteristics of the chassis and LRUs:

a. Chassis Assembly (MDP): EMI−designed to be housed in a standard 19−inch NASA rack. Its physical characteristics are: 12.22 +0.00/−0.03 inches in height, 17.75 inches maximum chassis width (including slides), 24 inches maximum depth, with a total weight more than 35 pounds and not to exceed 70 pounds. The MDP makes use of VME double−height printed wiring assemblies (PWAs), RF modules with front panel SMB

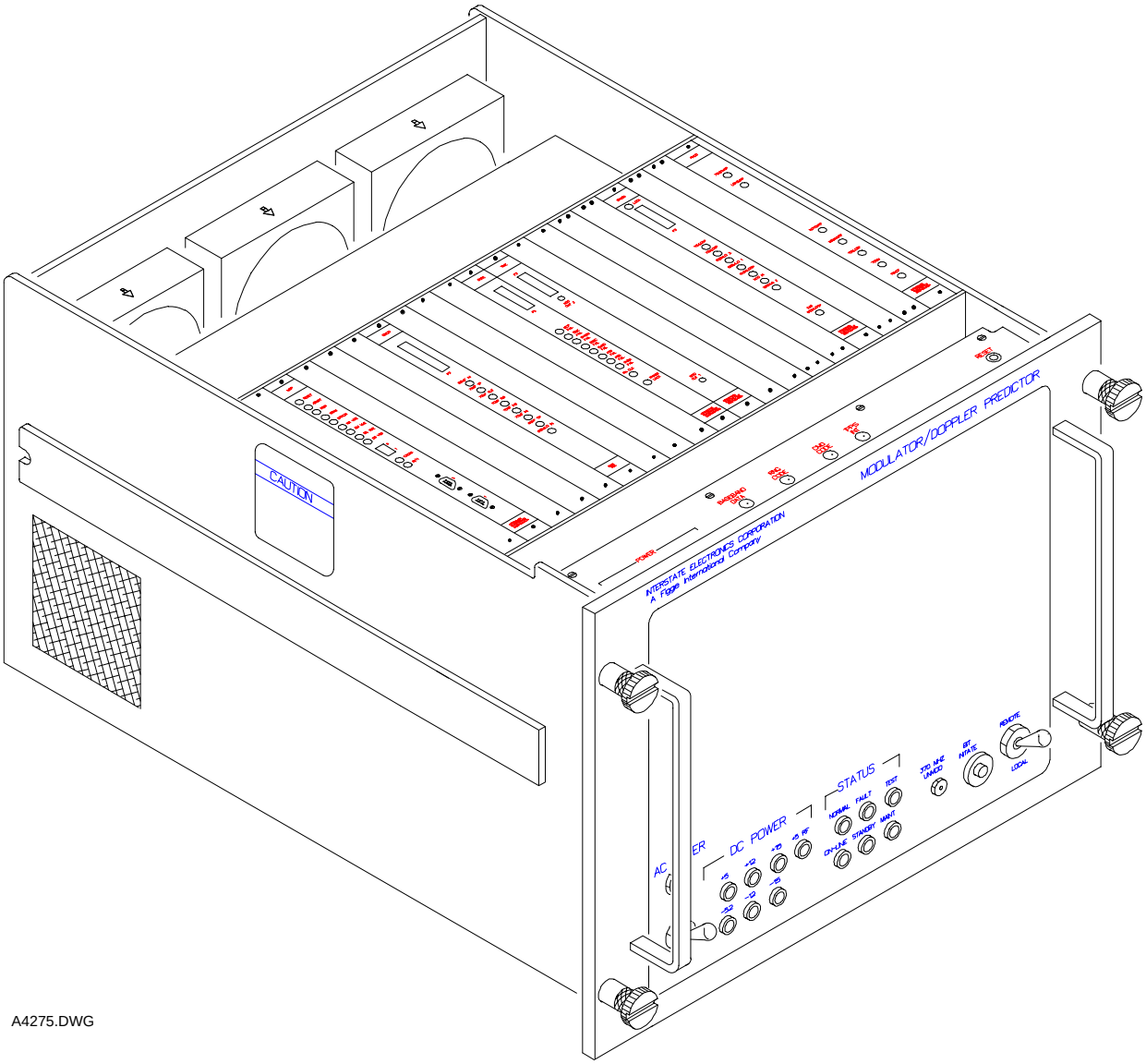


Figure 1—1. Modulator/Doppler Predictor P/N 7472300

coaxial and DIN 41612 type M, 60 contact connectors and 4 RF connectors, modular power supplies, and a common baseplate allowing for all internal PWA and RF module (non—RF) interfaces.

b. Power Supply No. 1 (PS1): 4.875” x 7.75” x 12.25” screw—mounted, terminal board wire connections, fan—cooled, 12 pounds maximum, LAMBDA LFQ series power supply.

c. Power Supply No. 2 (PS2): 2.5” x 4.9” x 14.0” screw—mounted, terminal board wire connections, 5.5 pounds maximum, convection—cooled multi—output power supply.

Table 1−2. Major Components		
COMPONENT	REFERENCE DESIGNATOR	FIGURE NUMBER
Modulator/Doppler Predictor	1	1−1
Power Supply No. 1	1A2	6−3−3
Power Supply No. 2	1A3	6−3−2
Modem Control Processor PWA	1A4A1	6−1−4
Data Conditioning and Encoding PWA	1A4A9	6−1−3
Timing Generator PWA	1A4A10	6−1−2
Synthesizer PWA	1A4A15	6−1−5
Forward Modulator PWA	1A4A18	6−1−6

d. Modem Control Processor (MCP) PWA: 9.2” x 6.3” printed wiring assembly, screw−mounted, VME double−height, dual 96−pin DIN 41612 connectors, front panel mounted LEDs and switches for status/control, and dual front panel mounted RS−232/RS−422/RS−485 interface selectable (9−pin) connectors. Utilizes four plug−in sockets to house the latest MCP/Exec firmware release IC chip set; SP7472300−xxx (J21, J23, J25, and J27) where xxx represents the released version. Refer to the label on the inside of the unit top cover for applicable released version.

e. Data Conditioning and Encoding (DCEC) PWA: 9.2” x 6.3” printed wiring assembly, screw−mounted, VME double−height, dual 96−pin DIN 41612 connectors, and front panel mounted LEDs, SMB coaxial connector, and a 40−pin test point connector.

f. Timing Generator (TIME) PWA: 9.2” x 6.3” printed wiring assembly, screw−mounted, VME double−height, dual 96−pin DIN 41612 connectors, front−panel−mounted dual SMB coaxial connectors and a 40−pin test point connector.

g. Synthesizer (SYNTH) PWA: 9.2” x 6.3” printed wiring assembly, screw−mounted, VME double−height, dual 60−pin DIN 41612 type M connectors with four RF connectors each, front−panel−mounted LED, SMB coaxial connectors (seven), and a 40−pin test point connector.

h. Forward Modulator (FMOD) PWA: 9.2” x 6.3” printed wiring assembly, screw−mounted, VME double−height, dual 60−pin DIN 41612 type M connectors with four RF connectors each and front−panel SMB coaxial connectors (five).

i. Ground Network Modulator (GMOD) PWA: 9.2” x 6.3” printed wiring assembly, screw−mounted, VME double−height, dual 96−pin DIN 41612 connectors, SMB coaxial connectors, and a 50−pin test point connector.

1−3 Functional Description

This paragraph provides a brief functional description of the chassis and each Level 1 LRU. Items covered include the overall functions of the chassis unit as a whole and then each LRU as it applies to pertinent input/output signals.

1−3.1 MDP Chassis Assembly

The MDP is used interchangeably in the KSA low data rate (LDR) equipment, SSA equipment, or MA receiver/transmit equipment. The MDP interfaces with the SSA, KSA, and MA control hardware configuration items (HWCIs) and common time and frequency system (CTFS) in the SSA, KSA, and MA portions of the Forward USS

RF equipment groups, respectively, and other configuration items (when applicable), in the subsystem in which it is utilized. Figure 1 - 2 shows the SSA and MA interface configuration, and figure 1 - 3 shows the KSA low data rate interface configuration. The following paragraphs provide simplified functional and interface information for the MDP LRUs; refer to figure 4 - 1 for the functional block diagram.

1—3.2 Power Supply No. 1

PS1 accepts the 120 - Vac site - supplied power and outputs regulated +5.0 Vdc, +5.0 RF Vdc, and +/ - 15.0 Vdc source power for circuits throughout the MDP.

1—3.3 Power Supply No. 2

PS2 accepts the 120 - Vac site - supplied power and outputs regulated - 5.2 Vdc and +/ - 12.0 Vdc source power for circuits throughout the MDP.

1—3.4 Modem Control Processor PWA

1—3.4.1 MCP Functions — The MCP provides the required computations, scheduling of events, and overall control of MDP operations via the VMEbus. The MCP provides the following:

a. A 68030 central processing unit (CPU) operating at 25 MHz.

b. Capability of up to 5 mega - instructions per second (MIPS) through the 1 - Mbyte on-board static random access memory (SRAM) and the on - chip cache.

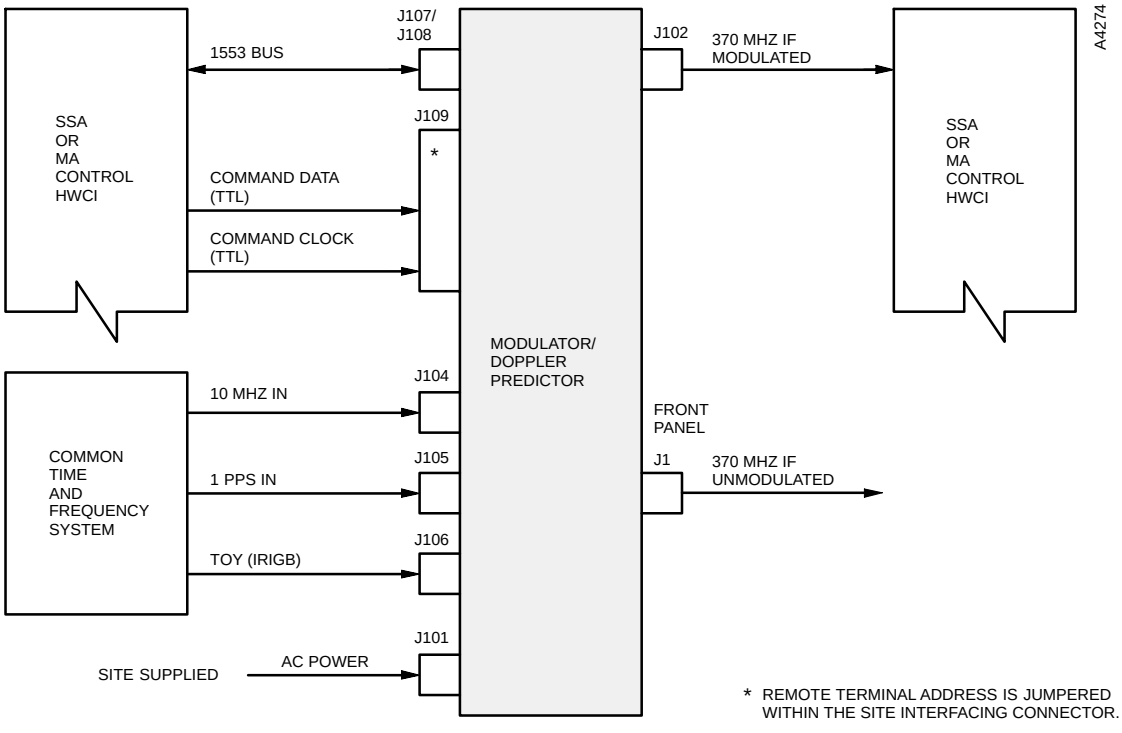


Figure 1—2. Modulator/Doppler Predictor Interfaces for the MA Receiver/Transmit and SSA Equipment Configurations

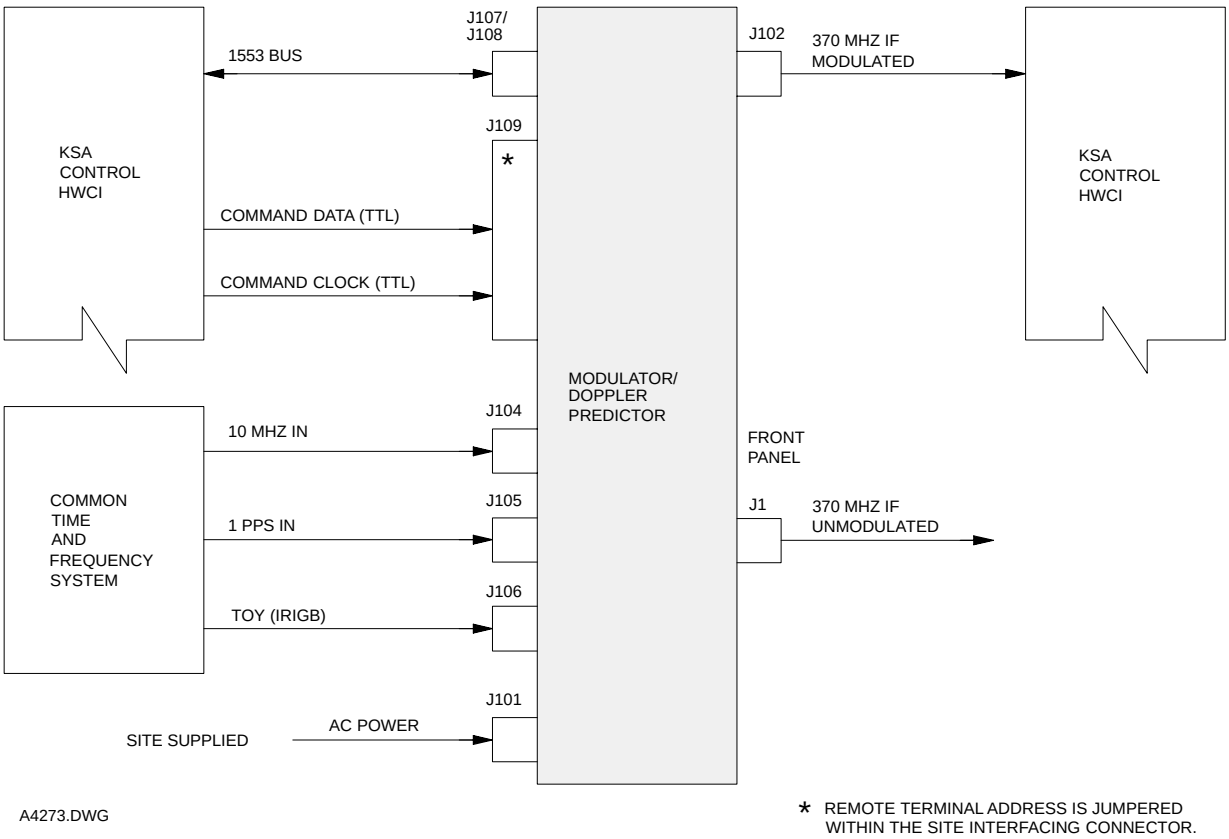


Figure 1−3. Modulator/Doppler Predictor Interfaces for the KSA Low Data Rate Equipment Configuration

c. Two 68561 multiprotocol communications controllers (MPCCs) for serial I/O (RS−232 compatible interface with one channel−selectable RS−232/ RS−422/ RS−485).

d. Two parallel interface and timer (PI/T) devices for local control, interrupt level control, and timer functions.

e. Two 68153 bus interrupter modules (BIMs) for all local interrupts.

1−3.4.2 MCP Interfaces − MCP provides the following interfaces:

a. DCEC (via VMEbus) to provide control of the data format conversion, convolutional encoding, symbol format conversion, PN code generation, and transition density monitoring.

b. TIME (via VMEbus) to provide control of the 1553 MDP interface, IRIG−B data, NCO, and VMEbus access to various timing, voltage, temperature and epoch measurements.

c. GMOD (via VMEbus) to provide control of data format conversion and other baseband processing, and to provide control of the modulation configuration for all GN modulation formats.

1−3.5 Data Conditioning And Encoding PWA

1−3.5.1 DCEC Functions − DCEC provides the following functions:

a. Data format conversion (command data channel): NRZ−L to NRZ−M or NRZ−S and NRZ−L to biphase−L.

b. Convolutional encoding (rate 1/3, K = 7 encoding, nontransparent).

c. Symbol clock synchronization with data clock: synchronize 6x data clock with the input data clock (supported for S−Shuttle modes 1 and 2 rates only).

d. Symbol format conversion: NRZ to biphase conversion (applied after encoder, supported for S - Shuttle modes 1 and 2 rates only).

e. PN spreading: PN spreading for command and range channels, PN code generation, external PN clock input (from TIME), and epoch synchronization with 1 PPS.

f. Clock detection: detect if clock rate is less than 97 Hz.

g. Data presence check: detect any data transition between data presence status checks (VMEbus read of DCEC status register).

h. VMEbus interface: control registers for onboard and offboard functions, status registers for board status, and built - in test (BIT) status LEDs.

1—3.5.2 DCEC Interfaces — DCEC provides the following interfaces:

a. FMOD: DCEC provides range channel data, command channel data, and signal modulation control.

b. TIME: DCEC accepts timing signals (1000 PPS and PN code NCO) and provides PN code epochs.

c. MCP: DCEC (via the VME bus) accepts configuration/operation control data and provides status data.

1—3.6 Timing Generator PWA

1—3.6.1 TIME Functions - TIME provides the following functions: alignment of internal timing with CTFS supplied 1 PPS, time - of - year (TOY) data from the input IRIG - B signal, timing and epoch interrupts, time transfer measurement (epoch count), communicates with the VMEbus via a MIL - STD - 1553 interface, epoch status interface between DCEC and VMEbus, two numerically controlled oscillators (NCOs), power source measurements, and MDP front panel interface with VMEbus.

1—3.6.2 TIME Interfaces - TIME provides the following interfaces:

a. Time - of - year (seconds, minutes, Hours, and days) information to the VMEbus from the externally input serial IRIG - B data.

b. A controlled MIL - STD - 1553B interface with the VMEbus.

c. DCEC: TIME provides timing signals (1000 PPS and PN code NCO) and accepts PN code epochs.

d. Timing and epoch interrupts to the VMEbus from the 1 PPS, epoch, 50 - MHz signals and accept masking of any or all of these interrupts. An epoch count to the VMEbus. The epoch count is defined as the number of 10 - MHz clocks between the 1 PPS and the epoch mark.

e. FMOD: TIME accepts automatic level control (ALC) analog signals which are digitized and provided to the VMEbus. The ALC signals are for the 370 MHz modulated and unmodulated IF outputs.

f. SYNTH: TIME provides an NCO output that is MCP controlled (via VMEbus).

g. Output digitized voltage measurements to MCP (via VMEbus upon command) of the analog ALC signals from FMOD and various power sources.

h. A register that is capable of being observed at test points on the P3 connector and is controllable by the MCP. A driver register that interfaces the VMEbus and P2 connector.

1—3.7 Synthesizer PWA

1—3.7.1 SYNTH Functions — SYNTH uses phase - locked loops (PLLs) and divider circuits to generate the necessary clocks and timing signals needed by the MDP circuits. SYNTH uses the 10 - MHz input from the common time and frequency system (CTFS) to ensure system phase synchronization. SYNTH also provides an LED indicating the 61.5 - MHz PLL is locked, the 140 - MHz PLL is locked, and the 10 - MHz reference signal is present.

1−3.7.2 SYNTH Interfaces − SYNTH interfaces with the following:

a. FMOD: SYNTH provides the 300−MHz local oscillator (LO) and 70−MHz LO upconversion signals.

b. FMOD: SYNTH provides a 50−MHz clock and PLL status signals and accepts a compensated 20−MHz carrier NCO base timing signal.

c. External interface to accept the 10−MHz reference signal for synchronization and generation of MDP timing and clock signals.

1−3.8 Forward Modulator PWA

1−3.8.1 FMOD Functions − FMOD provides the necessary modulation functions for both the low data rate mode (rates less than or equal to 300 kbps) and high data rate (HDR) mode (rates greater than 300 kbps). Outputs both modulated and unmodulated 370−MHz IF and respective ALC signals.

1−3.8.2 FMOD Interfaces − FMOD interfaces with the following:

a. DCEC: FMOD accepts range channel data, command channel data, and signal processing control.

b. SYNTH: FMOD accepts both the 300−MHz and 70−MHz LO signal processing frequencies.

c. TIME: FMOD provides modulated and unmodulated ALC signals for analog−to−digital (A/D) conversion and monitoring.

d. GMOD: FMOD provides a 70 MHz IF signal for selection as signal to be upconverted for output.

e. GMOD: FMOD accepts a 70 MHz IF signal to be upconverted for 370 MHz IF output.

1−3.9 Ground Network Modulator PWA

1−3.9.1 GMOD Functions − GMOD provides the necessary functions to support the following GN modulation formats: Sinewave Subcarrier, Squarewave Subcarrier, and Direct Phase Modulation (with residual carrier) by PCM encoded forward data. The GMOD provides the following functions:

a. Data format conversion (command data channel): NRZ−L to NRZ−M, NRZ−S, biphase−L, biphase−M, or biphase−S.

b. Synchronization of data with subcarrier (when applicable).

c. Clock detection: Detect if input clock is present; for generation idle pattern, if selected.

d. VMEbus interface: Control registers for onboard functions and status registers for board status.

1−3.9.2 GMOD Interfaces − GMOD interfaces with the following:

a. SYNTH: GMOD accepts the 61.5 MHz LO signal processing frequency.

b. FMOD: GMOD accepts a 70 MHz IF signal from the FMOD.

c. FMOD: GMOD provides a 70 MHz IF signal to the FMOD to be upconverted to 370 MHz; this signal is either the same 70 MHz IF signal received from the FMOD, or it is a 70 MHz IF signal generated by the GMOD.

d. TIME: GMOD accepts a 50 MHz clock, used as the sample clock in its waveform synthesis.

1−4 Condensed Data

As applicable, refer to the following tables for MDP Level 1 maintenance:

a. Table 1−3, Electrical Characteristics; this table lists all input/output electrical characteristics of the MDP chassis and Level 1 LRUs.

b. Table 1−4, NASA Drawings; this table lists all MDP chassis and Level 1 LRU technical illustrations contained in sections 1 and 5 that have NASA drawing numbers assigned.

c. Table 1−5,Environmental Requirements; this table lists environmental conditions that MDP will not suffer permanent degradation or damage when subjected to.

d. Table 1−6, Equipment Required, but Not Supplied; this table lists all equipment required for MDP Level 1 maintenance, but not supplied with the unit.

e. Table 1−7, Consumables; this table lists all required consumables for MDP Level 1 maintenance.

Table 1−3. Electrical Characteristics

PARAMETER	DESCRIPTON
PHYSICAL CHARACTERISTICS	
Panel height	12.22, +0.00/−0.03 inches
Panel width	18.97, +0.00/−0.03 inches
Chassis depth	24 inches, maximum
Chassis width	17.75 inches, maximum (including slides)
Weight	70 pounds, maximum
POWER REQUIREMENTS	
Voltage	120 Vac; +/− 10% voltage regulation, single phase
Frequency	60 +/−3 Hz
Transients	+/− 15% of nominal voltage; surge for less than 0.5 second
Power consumption	350 watts, maximum
Panel connectors	Rear panel: 1A1J101, AC connector
370−MHz MODULATED IF OUTPUT	
Nominal frequency	370 MHz
Reference bandwidth	50 MHz
Output VSWR	Less than 1.3:1 over the reference bandwidth
Level	−10 dBm, +/−3 dBm
Stability of output power level	+/−1 dB over any 1−hour period over specified operating conditions
Spurious signals, total	Better than −35 dBc total in the nominal band width with no single spurious signal greater than −40 dBc
Panel connectors	Rear panel: 1A1J102, SMA
370−MHz UNMODULATED IF OUTPUT	
Nominal frequency	370 MHz
Reference bandwidth	5 MHz, minimum
Level	−15 dBm, +/−3 dBm
Stability	+/−1 dB over any 1−hour period over specified operating conditions
Output VSWR	Less than 1.3:1 over the reference bandwidth
Spurious signals, total	Better than −35 dBc total in the nominal bandwidth with no single spurious signal greater than −40 dBc
Panel connectors	Front panel: 1A7J1, SMA

Table 1−3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
CTFS INPUTS	
10 MHz	
Frequency	10 MHz
Waveform	Sinusoidal
VSWR from CTFS HWCI	1.1:1, maximum in a bandwidth from 9.75 MHz to 10.25 MHz
Impedance	50 ohms
Level	1.15 VRMS, +/− 15%
Single sideband phase noise	Better than −140 dBc for 1 kHz offset measured in a 1 Hz bandwidth
Accuracy	$+/-4.0 \times 10^{-12}$
Stability	$+/-8.5 \times 10^{-13}$ long term (100 seconds), $+/-5.0 \times 10^{-12}$ short term, (1 second)
Input VSWR	Better than 1.3:1 in a bandwidth from 9.5 MHz to 10.5 MHz
Panel connectors	Rear panel: 1A1J104, SMA
1 PPS	
Frequency	1 Hz
Waveform	Rectangular pulse
Impedance	50 ohms
Level	TTL levels
Pulse width, t_w	100 microseconds, +/−0.1%
Rise and fall times	< 10 nanoseconds
Jitter	< 2 nanoseconds
Accuracy	< +/−25.0 nanoseconds referenced to the CTFS master epoch
SWR	1.3:1 (1−35 MHz)
Panel connectors	Rear panel 1A1J105, SMA
Time of Year (TOY)	
Signal format	IRIG−B level shift
Impedance	50 ohms, nominal
Levels	TTL into 50 ohms
Panel connectors	Rear panel: 1A1J106, SMA

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
1553 BUS	
Description	MIL—STD—1553B Digital Time Division Command Response Multiplex Data Bus with the MDP configured as a remote terminal. Refer to ICD STGT—HE—06—2; GES—STGT—0004 for interface configuration and control information.
Mode	Single channel, redundant
Coupling	Transformer coupled
Remote terminal address	See table 4—3
Parity	Odd
Panel connectors	Rear panel: 1A1J107, 1A1J108 Twinax (threaded)
COMMAND DATA/CLOCK	
Format	NRZ
Data Rate	100 bps — 25 Mbps
Clock Rate	Same as data and synchronous with the data
Type	Complementary balanced differential TTL
Levels	Similar to RS—422A, extends to 25 MHz
Clock Asymmetry	50 +/—5 percent, maximum
Differential (A) to (B) voltage for clock or data	2.0 volts, minimum
Time Skew (A) to (B) for clock or data	6.5 nanoseconds, maximum
Time Skew (A) to (A) and (B) to (B) for clock data relative to data	25 percent of a bit period, maximum
20 to 80 percent differential time for clock or data	12 nanoseconds, maximum
Nominal Source Impedance	Less than 10 ohms
Input Impedance	100 ohms +/—2 percent line—to—line for each differential pair
Panel connectors	Rear panel; 1A1J109, 37—pin male D type

Table 1–3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
TIMING GENERATOR PWA	
Power consumption	43 watts, maximum; 33 watts, typical
Input power	+5.00 +/–0.25 Vdc; 5.4 ampere, maximum; 5.0 amperes, typical –5.2 +/–0.25 Vdc; 1.5 ampere, maximum; 0.75 ampere, typical +12.0 +/–1.2 Vdc; 1 milliampere, maximum; 1 microampere, typical –12.0 +/–1.2 Vdc; 1 milliampere, maximum; 1 microampere, typical +15.0 +/–1.5 Vdc; 0.2 ampere, maximum; 0.1 ampere, typical –15.0 +/–1.5 Vdc; 0.2 ampere, maximum; 0.1 ampere, typical
Logic inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc ECL Logic 0: –1.5 to –1.9 Vdc ECL Logic 1: –0.6 to –1.3 Vdc
Differential inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum 1553: 20 volts p–p, maximum
Logic outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc ECL Logic 0: –1.5 to –1.9 Vdc ECL Logic 1: –0.6 to –1.3 Vdc
Differential outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum 1553: per MIL–STD–1553
RF outputs	Frequencies of 8.5 +/–0.25 MHz and 20 +/–1.6 MHz with a 50 ohm nominal impedance and a +/–3.0 dBm output
SYNTHESIZER PWA	
Power consumption	37 watts, maximum
Input power	+5.00 +/–0.25 Vdc; 0.75 ampere, maximum –5.2 +/–0.25 Vdc; 0.75 ampere, maximum +15.0 +/–0.5 Vdc; 1.75 amperes, maximum –15.0 +/–0.5 Vdc; 0.2 ampere, maximum
Logic inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
SYNTHESIZER PWA (Continued)	
Logic outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc ECL Logic 0: −1.85 to −1.63 Vdc ECL Logic 1: −0.98 to − 0.81 Vdc
FORWARD MODULATOR PWA	
Power consumption	23.25 watts, maximum
Input power	+5.00 +/−0.25 Vdc; 0.3 ampere, maximum −5.2 +/−0.25 Vdc; 0.3 ampere, maximum +15.0 +/−0.5 Vdc; 1.0 ampere, maximum −15.0 +/−0.5 Vdc; 0.35 ampere, maximum
Logic inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential inputs	TTL: 0.7 Vdc ECL: 0.7 Vdc
Logic outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential outputs	TTL: 2.0 Vdc ECL: 0.8 Vdc
DATA CONDITIONING AND ENCODING PWA	
Power consumption	23.5 watts, maximum
Input power	+5.00 +/−0.25 Vdc; 0.8 ampere, maximum −5.2 +/−0.25 Vdc; 0.5 ampere, maximum +15.0 +/−0.5 Vdc; 0.8 ampere, maximum +12.0 +/−0.25 Vdc; 0.5 ampere, maximum −12.0 +/−0.25 Vdc; 0.5 ampere, maximum
Logic inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential inputs	TTL: 0.7 Vdc ECL: 0.7 Vdc
Logic outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential outputs	TTL: 2.0 Vdc ECL: 0.8 Vdc

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTON
POWER SUPPLY NO. 1	
AC input	95—132 Vac at 47—440 Hz; input power at maximum output power 633 watts
Efficiency	75% minimum at maximum output power
Inrush limiting	75 amperes maximum
EMI suppression	FCC Docket 20780, Class A and VDE 0871, Class A
Output voltage	+5.00 +/—0.25 Vdc, adjustable; 75, 66, and 57 amperes maximum at 40, 50, and 60 degrees Celsius, respectively. Minimum preload of 19.0 amperes is required on +5 Vdc output for maximum current on auxiliary outputs.
	+15.00 Vdc +/—0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit respectively.
	—15.00 Vdc +/—0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit, respectively.
	+5.00 RF Vdc +/—0.25 Vdc, adjustable; 7.5, 6.7, and 6.0 amperes maximum at 72, 90, and 108 degrees Fahrenheit, respectively.
Output power	475, 420, and 362 watts maximum at 72, 90, and 108 degrees Fahrenheit, respectively.
POWER SUPPLY NO. 2	
AC input	90—132 Vac at 47—63 Hz
Efficiency	65% to 75%
Inrush limiting	65 amperes maximum peak with electronic soft—start (150 amperes on 220 watts)
EMI suppression	FCC Docket 20780, Class A and VDE 0871, Class A
Output voltage	—5.20 +/—0.25 Vdc, adjustable; 30.0 amperes, maximum; 25 amperes, typical
	+12.00 +/—0.25 Vdc, adjustable; 5.0 amperes, maximum; 4.0 amperes, typical
	—12.00 +/—0.25 Vdc, adjustable; 6.0 amperes, maximum; 3.0 amperes, typical

Table 1—3. Electrical Characteristics (Continued)	
PARAMETER	DESCRIPTON
MODEM CONTROL PROCESSOR PWA	
Power Consumption	34 watts, maximum
Input Power	+5.00 +/—0.25 Vdc; 5.7 amperes, maximum +12.0 +/—0.25 Vdc; 0.2 amperes, maximum —12.0 +/—0.25 Vdc; 0.2 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc

Table 1—4. NASA Drawings		
DRAWING NO.	DESCRIPTION	PAGE
Not applicable.		

Table 1—5. Environmental Requirements

PARAMETER	DESCRIPTION
OPERATING ENVIRONMENT	
Temperature	+50 to +100 degrees Fahrenheit
Temperature rate	Temperature rate of change shall not exceed 10 degrees per hour
Humidity	From 20 to 80 percent without condensation
Altitude	Sea level to 12,000 feet
NONOPERATING ENVIRONMENT	
Temperature	−20 to +160 degrees Fahrenheit
Humidity	From 0 to 100 percent relative humidity, noncondensing environment
Altitude	Sea level to 35,000 feet
Solar Radiation	350 BTU/ft²/hour

Table 1—6. Equipment Required, but Not Supplied

MFR. MODEL/PART NO.	DESCRIPTION	PAGE
Not applicable.		

Table 1—7. Consumables

NOMENCLATURE	SPECIFICATION NUMBER/NSN	PART NO./CAGE	APPLICATION
Not applicable.			

1—5 Special Tools and Test Equipment

Table 1—8 lists and describes the special tools and test equipment required to maintain MDP only in the installed condition (Level 1 maintenance). All chassis—installed maintenance is performed using standard handtools. If any of the listed items are not available, equivalent part numbers may be used. The MDP is supported, as part of the Forward USS, by the performance measuring and monitoring (PMMS) test equipment (PTE) and maintenance test group (MTG). The PTE provides for preservice, post—maintenance, and end—to—end test (EET) verification of MDP and associated equipment. MTG provides control of test configuration, injection of test stimuli, measurements of equipment responses to stimuli, and displays results in a manner to permit failure localization.

Table 1—8. Special Tools and Test Equipment

RECOMMENDED MODEL/PART NO.	MANUFACTURER (FSCM/CAGE)	COMMON NAME	USE	FIG. NO.
5120—00—278—1267	81348	No. 1 flat—tipped screw—driver	Remove/replace LRUs	N/A
5120—01—022—9953	55719	No. 1 cross—tipped screw—driver	Remove/replace LRUs	N/A
6625—01—235—2911	89356	Multimeter	Measure voltages/ resistances	N/A
6966—C	78976	Gun, heat	Heat shrink—wrap	N/A
Commercial source		Vacuum cleaner	Clean unit interior	N/A
Commercial source		Snub—nosed pliers	Remove/replace lampholder, switch	N/A
Commercial source		IC chip puller	Remove/replace MCP IC chips	N/A
499—920—012	07421	Wirecutters/strippers	Remove/replace lampholder	N/A
499—925—014	07421	Soldering iron	Remove/replace lampholder	N/A
HP 5245A	Hewlett—Packard	Universal Counter	Measure frequency of RF signals	N/A

Section 2 — Installation

2–1 Introduction

This section contains chassis unpacking, installation, removal, packaging, and storage/shipment information for the Modulator/Doppler Predictor in STGT. This section also includes a detailed view of the rear panel and associated connectors, figure 2–1. Refer to table 4–3 for connector pin identification.

2–2 Chassis Installation In STGT

The MDP is a complete unit and requires no internal wiring, strapping, or cable changes other than factory setup. The unit is designed to be housed in the KSA low data rate equipment HWCI cabinet, SSA equipment HWCI cabinet, or MA receiver/transmit equipment HWCI cabinet; the rack numbers are: 1007, 1008, 1009, 1010, 1011, 1013, 1014, 1016, 1025, 1028, and 1122. All external cable and wiring interfaces are site supplied.

2–3 Unpacking

The MDP is shipped as a complete unit with all subassemblies (PWAs, power supplies, etc.) installed. The unit is wrapped in antistatic bubble–wrap material and placed in a shipping container as shown in figure 2–2. To unpack the unit, proceed as follows:

NOTE

Before unpacking the unit, inspect the shipping container for signs of external damage. If the container is damaged, notify the carrier as well as the authorized field service personnel.

Keep the shipping container for future use, storage, or shipment for service/repair. Refer to the repackaging for shipment and storage paragraphs later in this section.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

a. With the shipping container on the floor, topside up, open the shipping container by carefully cutting the plastic packing tape.

b. Remove the polyethylene packing material to gain access to the unit.

c. Remove the unit wrapped in antistatic bubble–wrap material. Remove the bubble–wrap from around the unit and place unit on floor (or other acceptable work area surface), topside up.

d. Perform a general inspection inventory of the major components (see table 1–2) to ensure the unit is complete.

2–4 Chassis Installation

WARNING

The MDP requires two people to safely lift and place/remove the unit into/from the cabinet assembly. Also, removing or installing items of equipment while the equipment cabinet is energized could result in damage to equipment or injury to personnel. Ensure that all power is removed from the equipment rack before attempting assembly.

The following procedure applies to all configurational uses of the MDP.

a. Remove all electrical power from the equipment cabinet where the unit is to be installed.

b. Gain access to the rear of the equipment cabinet assembly and ensure all cabling is clear for installation of unit.

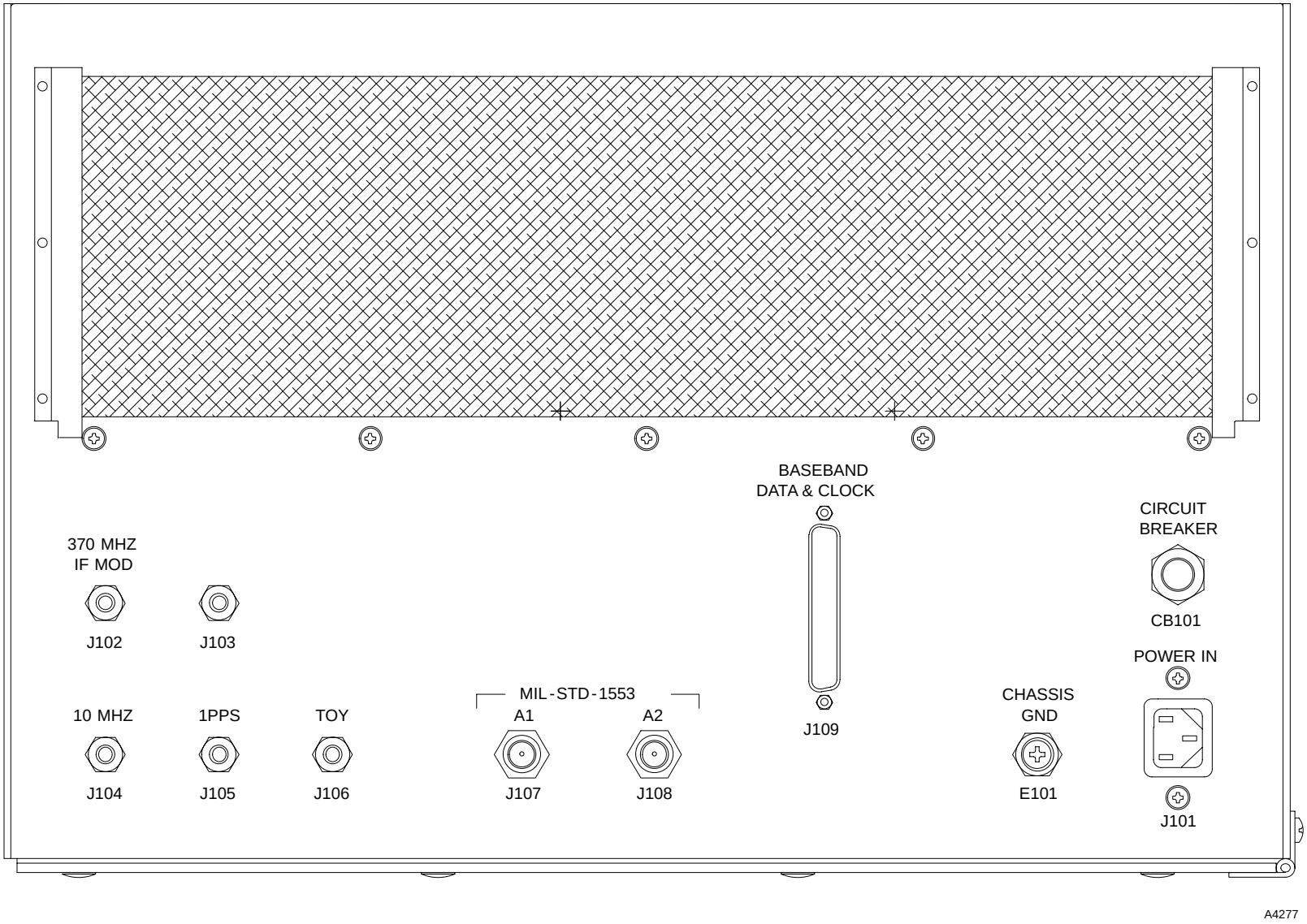


Figure 2—1. Modulator/Doppler Predictor Rear Panel

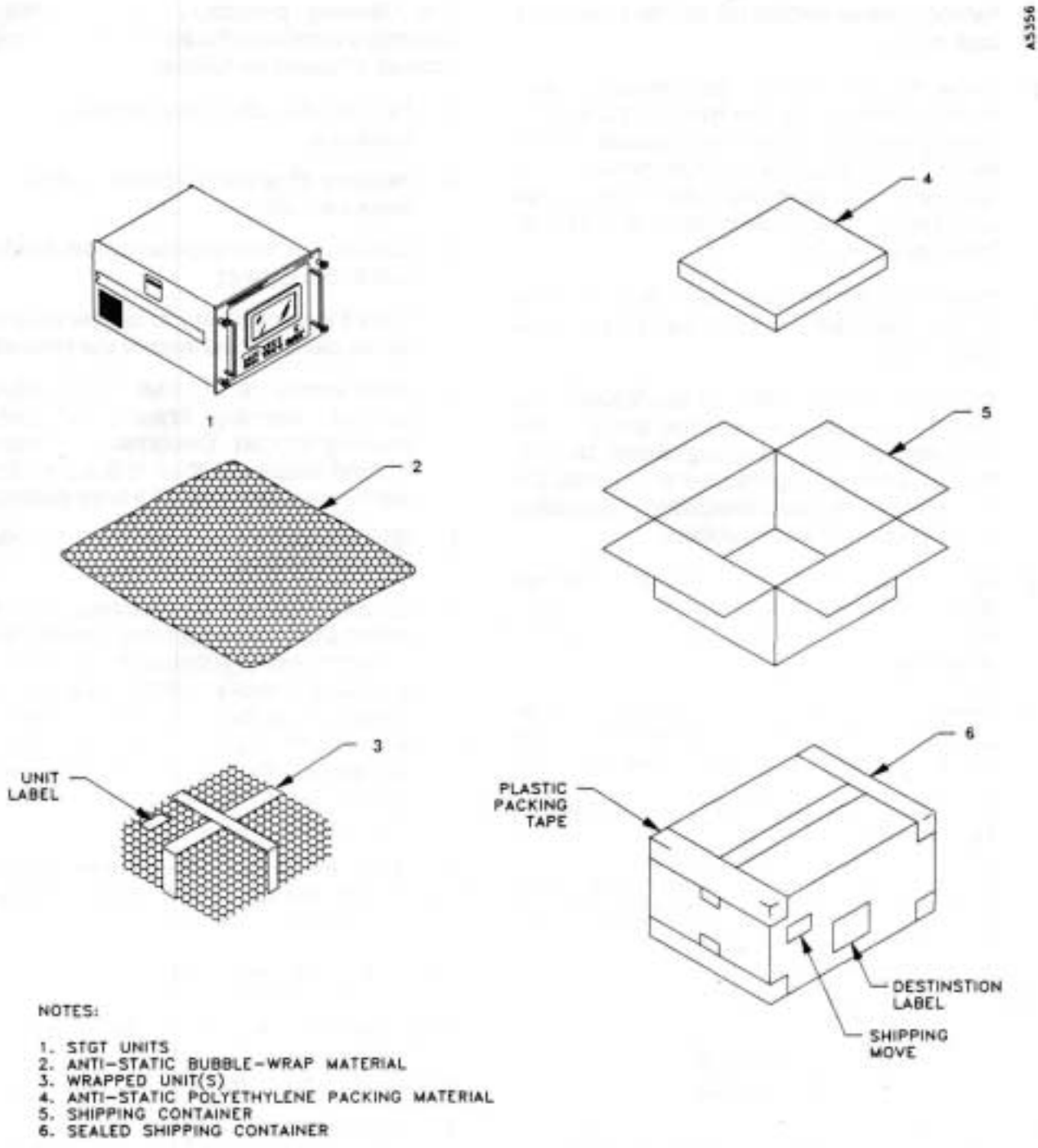


Figure 2—2. Equipment Packing/Unpacking

c. Extend cabinet section rail guides until guide lock seats.

d. Raise the unit (two people required), with each person placing one hand on front panel handle and the other hand placed underneath the unit; guide the unit section slide rails into their respective cabinet rail guides until the quick lock/disconnect mechanism locks into position.

e. Disengage the rail guide locks and slide unit slowly into equipment cabinet to ensure a clear entry.

f. At rear of cabinet, attach all applicable cable connectors (use finger force on all SMA connectors) and grounding straps to unit. Refer to section 1, figures 1—2 or 1—3, and site cable interfacing documentation, depending upon applicable configuration.

g. At the front of the unit, use a flat—tipped (common) screwdriver to tighten the four front—panel captive screws to the cabinet assembly.

h. Make a visual inspection to ensure that no cables are being pinched and that the unit is properly seated within the cabinet assembly.

i. Apply power to the cabinet assembly and all cabinet assembly units.

j. Perform the turn—on and self—check procedures found in section 3 to verify proper unit operation.

2—5 Chassis Removal

WARNING

The MDP requires two people to safely lift and place/remove the unit into/from the cabinet assembly. Also, removing or installing items of equipment while the equipment cabinet is energized could result in damage to equipment or injury to personnel. Ensure that all power is removed from the equipment rack before attempting disassembly.

The following procedure describes the steps necessary to remove the MDP from the equipment cabinet. Proceed as follows:

a. Perform the shutdown procedure found in section 3.

b. Remove all electrical power from the equipment cabinet.

c. Loosen the four captive screws holding the unit in the cabinet.

d. Slide the unit forward to enable easy access to the cables at the rear of the chassis.

e. Gain access to the rear of the equipment cabinet assembly. Ensure that cables are properly tagged. Disconnect all cables and ground straps attached to the unit. Connect the 10—MHz cable to a 50 ohm dummy load.

f. Slide the unit forward until the rail guide locks are set to the locked position.

g. On each side of the unit, press the rail guide quick lock/disconnect mechanism and pull the unit forward just past the point where the mechanism locks. With two people, one on each side of the unit, placing one hand on front panel handle and the other hand underneath the unit, slide the unit out of the cabinet rail guides and place the unit on a workbench.

h. At the equipment cabinet, disengage the rail guide locks and slide the rail guides back into the cabinet.

2—6 Unit Packaging

The following procedure provides the necessary instructions to package the MDP for storage or shipment. Refer to figure 2—2.

a. Obtain a quantity of antistatic bubble—wrap material (Federal Specification PPP—C—795, class 2) sufficient to wrap the unit to a thickness of at least 3—1/2 inches. Material must be of 1/2—inch thickness, and multiple wrappings must add up to a minimum of 3—1/2 inches.

b. Wrap unit with bubble—wrap and secure with masking tape.

c. Fill out a unit container label per STDN No. 507, Network Logistics Manual which includes the following information:

   (1) National stock number or activity control Number

   (2) Part number

   (3) Part name

   (4) Serial number

   (5) Manufacturer's name

   (6) Quantity

d. Secure the label to the wrapped unit.

e. Place the maintenance report (when applicable) in an envelope. Identify on the envelope that it contains the maintenance report and attach the envelope to the unit.

f. Place unit in a cushioned shipping/storage container. The shipping/storage container should be in accordance with customer logistics procedures.

g. Place sufficient antistatic polyethylene packing material (type I) around the unit to ensure no movement during shipment.

h. Seal the container with plastic packing tape or other suitably strong tape.

i. Fill out a shipping label per STDN No. 507, Network Logistics Manual.

j. Place the shipping label in the upper left corner of the shipping container side.

k. Fill out the destination address label and place it in the center of the shipping container side.

2–7 PWA Packaging

The following procedure provides the necessary instructions to package a PWA for storage or shipment.

a. Obtain a quantity of antistatic bubble–wrap material (Federal Specification PPP–C–795, class 2) sufficient to wrap the PWA to a thickness of at least 1 inch. Material must be of 1/2–inch thickness, and multiple wrappings must add up to a minimum of 1 inch.

b. Wrap PWA with bubble–wrap and secure with masking tape.

c. Fill out a PWA container label per STDN No. 507, Network Logistics Manual which includes the following information:

   (1) National stock number or activity control Number

   (2) Part number

   (3) Part name

   (4) Serial number

   (5) Manufacturer's name

   (6) Quantity

d. Secure the label to the wrapped PWA.

e. Place the maintenance report (when applicable) in an envelope. Identify on the envelope that it contains the maintenance report and attach the envelope to the PWA.

f. Place PWA in a cushioned shipping/storage container. The shipping/storage container should be in accordance with customer logistic procedures.

g. Place sufficient antistatic polyethylene packing material (type I) around the PWA to ensure no movement during shipment.

h. Seal the container with plastic packing tape or other suitably strong tape.

i. Fill out a shipping label per STDN No. 507, Network Logistics Manual.

j. Place the shipping label in the upper left corner of the shipping container side.

k. Fill out the destination address label and place it in the center of the shipping container side.

2–8 Storage

2–8.1 Short–Term Storage

For short–term storage the unit suffers no permanent degradation or damage when stored under the following environmental conditions:

a. Temperature: −40 to 160 degrees Fahrenheit.

b. Humidity: 0 to 100 percent relative humidity, noncondensing environment.

c. Altitude: Sea level to 35,000 feet.

2−8.2 Long−Term Storage

For long−term storage repackage the unit up to step (g) of the packaging procedure in paragraph 2−6. The unit suffers no permanent degradation or damage when stored under the environmental conditions specified in paragraph 2−8.1.

2−9 Shipment

Package the unit/PWA for shipment according to the procedures in paragraph 2−6 or 2−7. Ship the packaged unit by best commercial method.

Section 3 — Operation

3–1 Introduction

This section contains information and procedures to aid personnel in operating and maintaining the Modulator/Doppler Predictor. A complete identification of all operating controls and indicators is included. Prior to performing maintenance, the paragraphs and procedures in this section must be understood and implemented.

WARNING

All personnel are required to read and understand paragraph 3–5, SAFETY, prior to performing any operations, removal/replacement, connections, and/or hardware tests on chassis. Failure to do so can cause death, injury, or equipment damage.

3–2 Modes Of Operation

The MDP has three operating modes: online, hot standby mode, and maintenance/software delivery (offline) mode. These modes are all remotely controlled. All three equipment modes are enabled when the front panel REMOTE/LOCAL switch is in the REMOTE position (remote control), and local control is enabled when the REMOTE/LOCAL switch is in the LOCAL position (local control). The MDP must be offline (front panel ONLINE indicator turned off and MAINT indicator turned on) in order to perform maintenance on the MDP. The offline condition can be enabled by the TDRSS Operations Control Center No. 2 (TOCC2) operator when remote control is active or by placing the REMOTE/LOCAL switch to the LOCAL position.

3–3 Remote Control

The normal operating mode of the MDP is remote control (front panel LOCAL/REMOTE switch placed in the remote position). Remote control of the MDP is handled by the automated data processing equipment (ADPE) interfaced to the MDP via the 1553 Bus. Refer to STGT USS TOCC2 operators manual for normal/maintenance operations of the MDP during remote control operation.

3–4 Local Control

Local control (offline mode) of the MDP is strictly a maintenance mode. By placing the LOCAL/REMOTE switch in the local position, an operator is enabling the extended (offline) BIT function to be initiated from the front panel. By placing the MDP in the local control condition, the unit cannot progress past the standby state (refer to section 4 for an explanation of the MDP states of operation). To perform maintenance operations on the MDP during local control, refer to section 5.

3–5 Safety

The following are warnings that are generally applicable when working near or inside equipment containing high voltage or other hazards that can cause death or injury and equipment damage. All warnings contained herein must be read and understood before proceeding with any removal/replacement, hardware tests, and/or connections on the MDP. Throughout this manual, specific warnings, cautions, and notes appear immediately before each paragraph or procedural step to which they pertain.

WARNING

USE EXTREME CAUTION WHEN PERFORMING THE PROCEDURES IN THIS MANUAL. Contact with energized circuits can cause personal injury or death. Personnel should be familiar with CPR. REMOVE RINGS, BRACELETS, WRISTWATCH, NECKCHAINS, AND OTHER METAL BEFORE WORKING AROUND ELECTRONIC/MECHANICAL EQUIPMENT. Jewelry can get caught and cause injury, or can cause a short circuit on contact and cause severe burns and electrical shock.

WHEN AN ABNORMAL CONDITION EXISTS AND PERTINENT PROCEDURES DO NOT APPLY, STOP THE MAINTENANCE ACTIONS AND OBTAIN EXPERT GUIDANCE. Failure to comply could lead to death or injury and equipment damage.

3−6 Equipment Access

To perform local control operations of the MDP, the unit must be extended to gain access to the maintenance panel. Loosen the four captive screws holding the unit in the cabinet. Slide the unit forward until the rail guide locks are set to the locked position.

3−7 Controls And Indicators

Before proceeding with any operation with the MDP, refer to paragraph 3−5. Figures 3−1 through 3−4 illustrate the various controls and indicators of the MDP. Tables 3−1 through 3−5 contain a complete list of the operating controls and indicators, including reference designators and brief functional descriptions.

3−8 Self−Check

Before proceeding with any operation of the MDP, refer to paragraph 3−5. The following procedures pertain to operating the MDP under local control maintenance conditions. Refer to STGT USS TOCC2 operators manual for normal and maintenance operating procedures performed from the TOCC2 console by the TOCC2 operator (remote control). Refer to the applicable O&M manual for maintenance procedures within suspect ambiguity group, but not accomplished by the TOCC2 operator (performed by the line maintenance technician (LMT) utilizing the maintenance test group (MTG)). The applicable STGT manual numbers and titles are:

a. MA Forward 0&M Manual; 530−STGT−O4006.

b. MA Return 0&MManual; 530−STGT−O4005.

c. SSA Forward 0&M Manual; 530−STGT−O4002.

d. KSA Forward 0&M Manual; 530−STGT−O4004.

3−9 Turn−On

The MDP requires no special actions to be taken when turning on a newly installed MDP assembly. Turn on the MDP by placing the ON/OFF switch in the ON position. Verify the AC POWER and DC POWER indicators turn on.

3−10 Built−In Test

The MDP employs three levels of self−check built−in test (BIT) features. The first−level BIT (confidence BIT) is performed at powerup and reset of the unit (see paragraph 3−15). The second−level BIT (online BIT) is performed continuously during all operational states of the MDP (see paragraph 3−16). The third−level BIT (extended BIT) is performed upon command (from ADPE in remote control or front panel (BIT INITIATE) in local control) (see paragraph 3−17). While in remote control, extended BIT can be commanded during any MDP operational state.

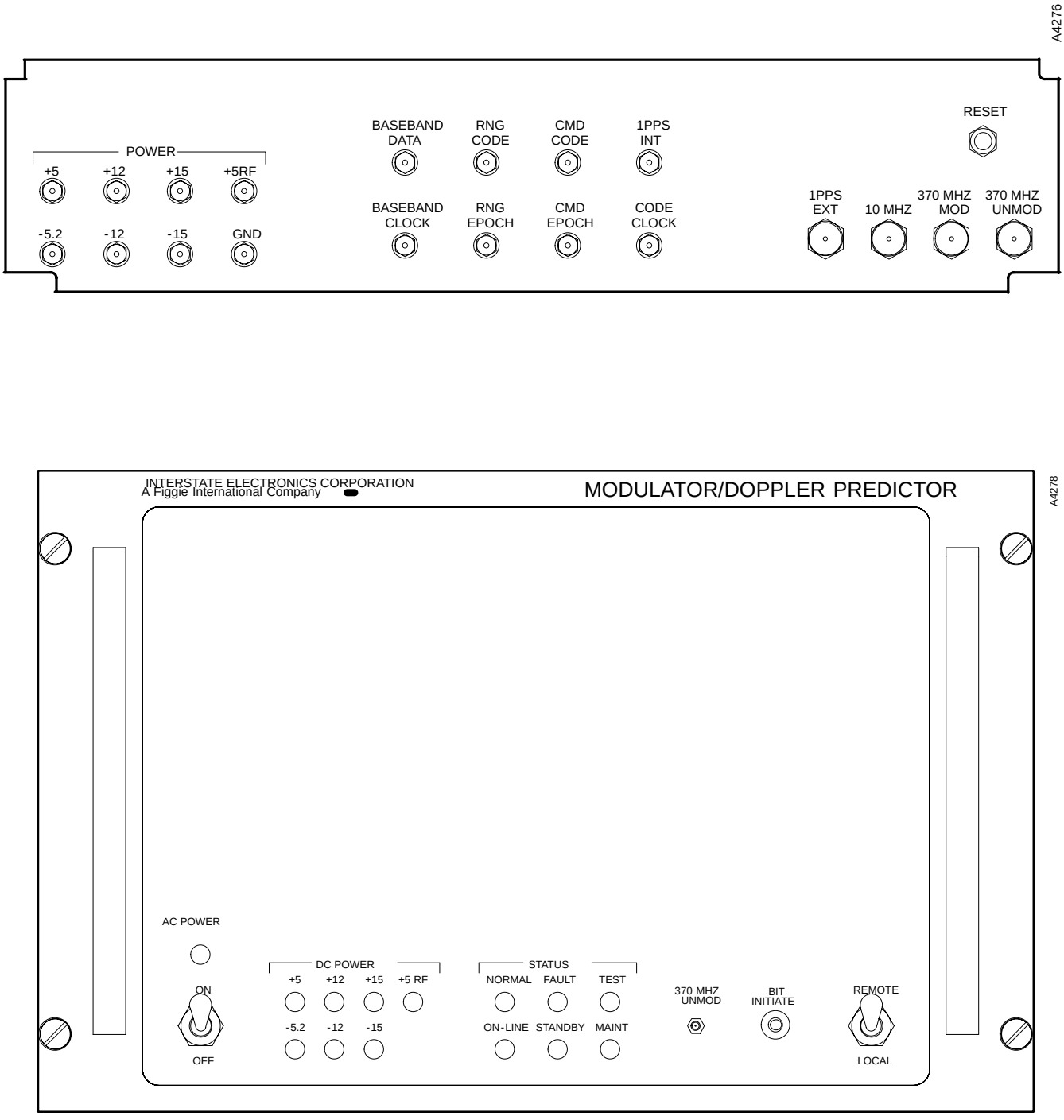
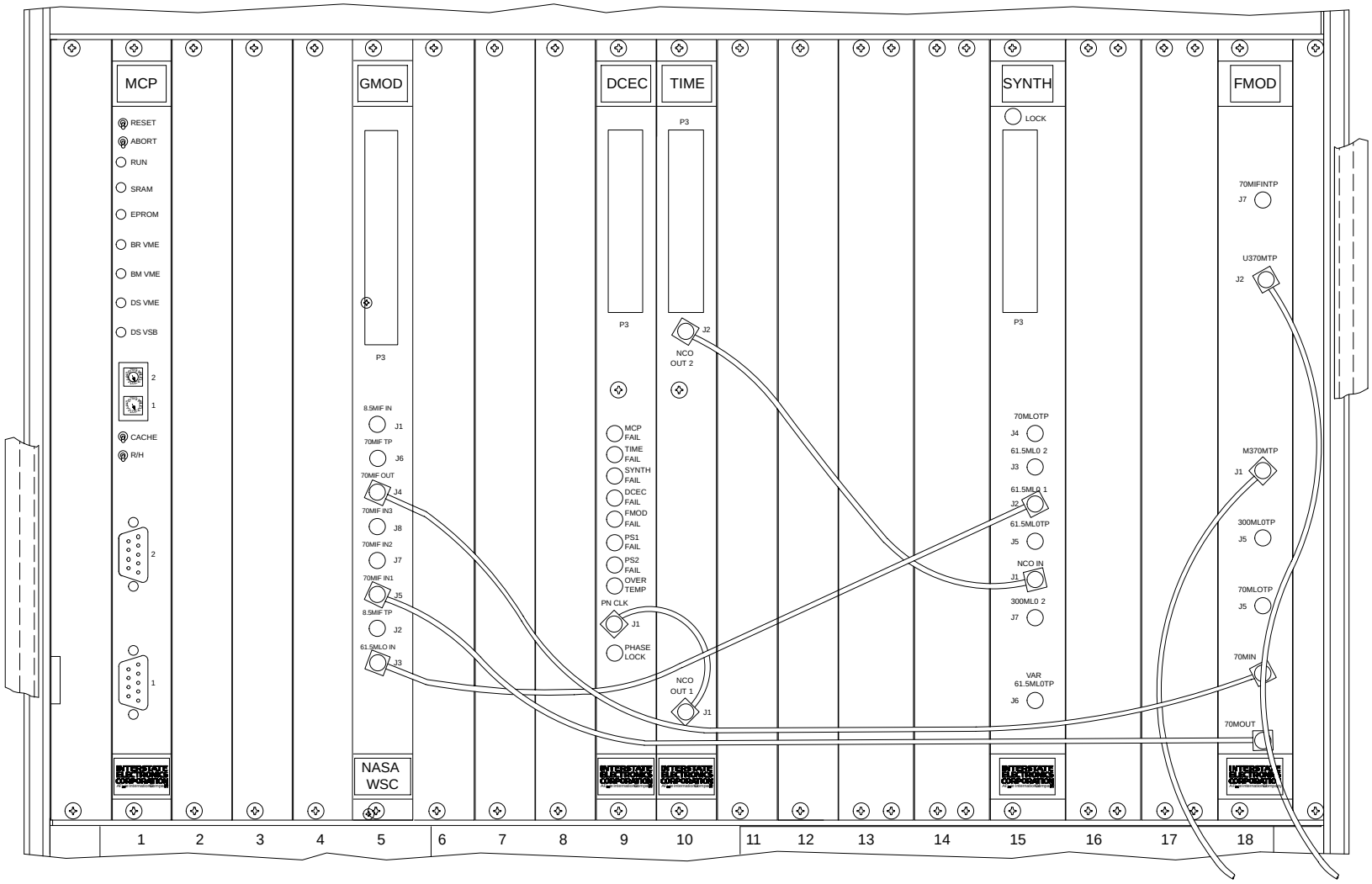
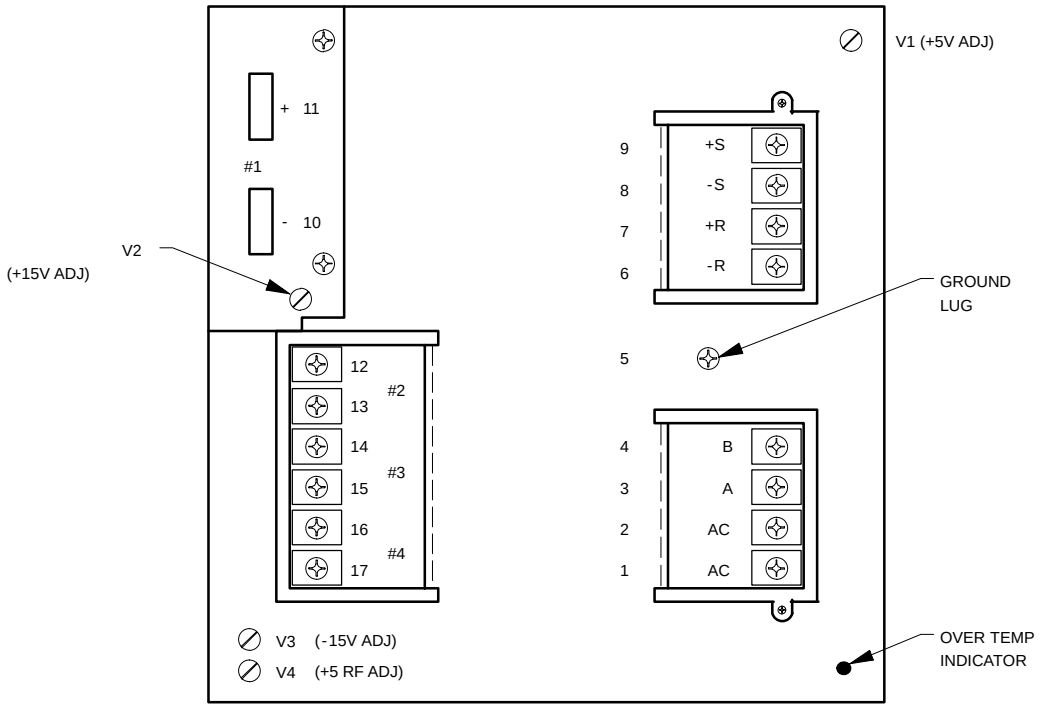


Figure 3 - 1. Modulator/Doppler Predictor Front and Maintenance Panel



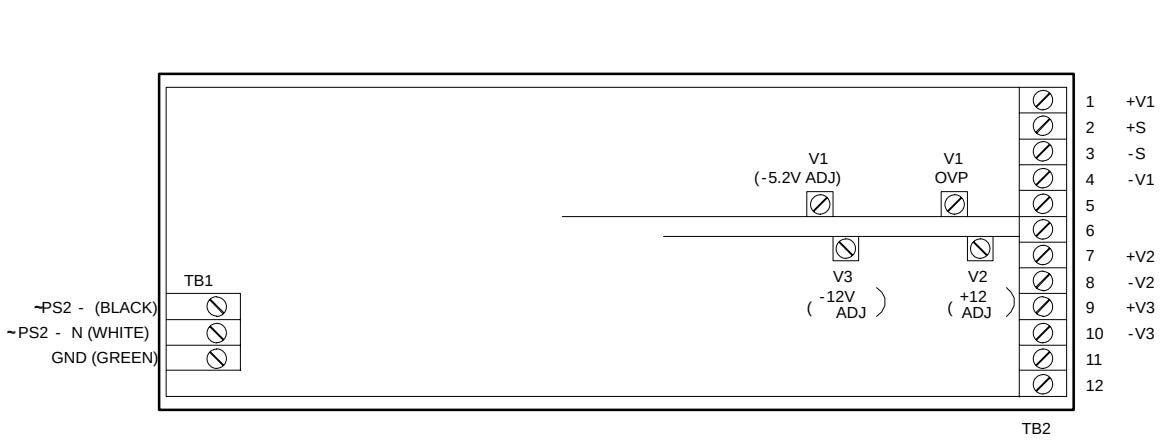
A4414–1.DWG

Figure 3–2. Modulator/Doppler Predictor PWA Front Panels



NOTE: POWER SUPPLY PS1 SHOULD HAVE A JUMPER STRAP FROM 3 TO 4.

Figure 3 - 3. Power Supply No. 1 Control and Indicators



NOTE: POWER SUPPLY PS2 SHOULD HAVE A JUMPER STRAP FROM TB2-1 TO TB2-2, AND TB2-3 TO TB2-4.

Figure 3 - 4. Power Supply No. 2 Controls

Table 3—1. Modulator/Doppler Predictor Front Panel Controls and Indicators				
FIG. REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3—1	AC POWER	1A7DS1	Indicator	Turns on green to indicate AC power has been distributed through unit
3—1	ON/OFF	1A7SW1	Toggle Switch	Primary power on/off control
3—1	DC POWER			
	+5	1A7DS2	Indicator	Turns on green to indicate +5 Vdc power supply is activated
	+12	1A7DS3	Indicator	Turns on green to indicate +12 Vdc power supply is activated
	+15	1A7DS4	Indicator	Turns on green to indicate +15 Vdc power supply is activated
	+5 RF	1A7DS5	Indicator	Turns on green to indicate RF +5 Vdc power supply is activated
	—5.2	1A7DS9	Indicator	Turns on green to indicate —5.2 Vdc power supply is activated
	—12	1A7DS10	Indicator	Turns on green to indicate —12 Vdc power supply is activated
	—15	1A7DS11	Indicator	Turns on green to indicate —15 Vdc power supply is activated
3—1	STATUS			
	NORMAL	1A7DS6	Indicator	Turns on green to indicate that the unit is in normal operation and has passed extended BIT or confidence BIT
	FAULT	1A7DS7	Indicator	Turns on red to indicate that the unit has detected a fault as a result of the confidence, extended, or online BIT
	TEST	1A7DS8	Indicator	Turns on amber to indicate that the unit is in process of performing extended BIT or confidence BIT

Table 3—1. Modulator/Doppler Predictor Front Panel Controls and Indicators (Continued)

FIG. REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3—1	STATUS (Continued)			
	ON—LINE	1A7DS12	Indicator	Turns on green when the Online Operational Light data item, received via the MIL—STD—1553 interface, is set
	HOT—STBY	1A7DS13	Indicator	Turns on green when the Standby Operational Light data item, received via the MIL—STD—1553 interface, is set
	MAINT	1A7DS14	Indicator	Turns on green when the Maintenance Operational Light data item, received via the MIL—STD—1553 interface, is set
3—1	370 MHZ UNMOD	1A7J1	Connector	Unmodulated 370—MHz IF output from FMOD; Signal contains all Doppler and carrier sweep effects
3—1	LOCAL/ REMOTE	1A7SW2	Toggle switch	LOCAL: Locks out the 1553 bus interface and allows the operator to command the extended BIT from the BIT INITIATE switch REMOTE: Locks out any operator control from the BIT INITIATE switch and enables unit control from the 1553 bus
3—1	BIT INITIATE	1A7SW3	Pushbutton switch	Initiates the MDP extended BIT routines when the MDP is in the local mode; Disabled when the MDP is in remote mode

Refer to section 5, paragraph 5—6 for procedures concerning initiation of MDP BIT functions while in the local control condition. Refer to STGT USS TOCC2 operations manual and TOCC2 operator for initiation of MDP BIT functions while in the remote control condition.

3—11 Normal Operation

Refer to STGT USS TOCC2 operators manual and TOCC2 operator for operating MDP during normal (remote control) conditions.

Table 3—2. Modulator/Doppler Predictor Maintenance Panel Controls and Indicators				
FIG. REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3—1	POWER			
	+5	1A6TP1	Test point	PS No. 1 generated +5 vdc signal
	+12	1A6TP2	Test point	PS No. 2 generated +12 vdc signal
	+15	1A6TP3	Test point	PS No. 1 generated +15 vdc signal
	—5.2	1A6TP4	Test point	PS No. 2 generated —5.2 vdc signal
	—12	1A6TP5	Test point	PS No. 2 generated —12 vdc signal
	—15	1A6TP6	Test point	PS No. 1 generated —15 vdc signal
	+5 RF	1A6TP7	Test point	PS No. 1 generated RF +5 vdc signal
3—1	GND	1A6TP8	Test point	Signal ground
3—1	BASEBAND DATA	1A6TP9	Test point	A buffered TTL version of the command channel input data
3—1	BASEBAND CLOCK	1A6TP10	Test point	A buffered TTL version of the command channel input clock signal
3—1	RNG CODE	1A6TP11	Test point	TTL version of the PN code for the MDP generated range channel
3—1	RNG EPOCH	1A6TP12	Test point	TTL version of the PN code epoch for the MDP generated range channel
3—1	CMD CODE	1A6TP13	Test point	TTL version of the PN code for the command channel
3—1	CMD EPOCH	1A6TP14	Test point	TTL version of the PN code epoch for the command channel
3—1	1PPS INT	1A6TP15	Test point	TIME generated 1—Hz TTL signal with a 20% duty cycle and valid on the falling edge; Based upon the 50—MHz signal input from the SYNTH PWA and the PPS external input

Table 3—2. Modulator/Doppler Predictor Maintenance Panel Controls and Indicators (Continued)

FIG. REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3—1	CODE CLOCK	1A6TP16	Test point	TTL version of PN code clock used for range and command PN code streams
3—1	RESET	1A6SW4	Pushbutton Switch	Switch activation initiates unit initialization and self—test features
3—1	1PPS EXT	1A6J5	Connector	Connector access to 1PPS external input
3—1	10 MHZ	1A6J1	Connector	Connector access to 10—Mhz reference frequency external input
3—1	370 MHZ MOD	1A6J2	Connector	Connector access to the modulated 370—MHz IF output from the FMOD; The signal is modulated with range and/or command channels; It does include all Doppler/sweep compensations
3—1	370 MHZ	1A6J3	Connector	Connector access to the unmodulated 370—MHz IF
3—1	UNMOD			output from the FMOD; The signal is not modulated but does have all Doppler/ sweep compensations

3—12 Emergency Operation

Refer to STGT USS TOCC2 operators manual and TOCC2 operator for operating MDP during emergency conditions.

3—13 Shutdown

Secure the MDP by placing the ON/OFF switch in the OFF position. Verify the AC POWER and DC POWER indicators turn off.

3—14 BIT Features

The MDP employs three levels of BIT features. Refer to the following paragraphs for explanations of the specific functions performed:

a. Confidence BIT: 3—15.

b. Online BIT: 3—16.

c. Extended BIT: 3—17.

3—15 Confidence Bit

The MDP runs initialization and self—test routines (confidence BIT) at powerup or unit reset. Upon initiation of the confidence BIT, the front panel

Table 3—3. Modulator/Doppler Predictor PWA Controls and Indicators

FIG. REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3—2	Modem Control Processor PWA	RESET	Switch	A reset of all onboard I/O devices and FPCP is enabled if the RESET switch is pushed to the “up” position; RESET s held active until the switch is in the “down” position; In addition, a local timer guarantees a minimum reset time of 2 to 3 seconds; Power fail and power up also force a reset (2—3 seconds) to start the board if the supply voltage is out of range (below 4.75 volts)
		ABORT	Switch	The ABORT switch, which provides an interrupt on a software—programmable level, is provided on the board to allow an abort of the current program, to trigger a self—test, or to start a maintenance program; ABORT is activated in the “up” position and deactivated in the “down” position
		RUN	Indicator	The RUN LED is green if the processor is not in the halt state; It is red during the reset phase or when the processor is in the halt state
		SRAM	Indicator	The SRAM LED is always lit yellow when the processor is accessing the local SRAM
		EPROM	Indicator	The EPROM LED is lit yellow when the processor accesses the EPROM area
		BR VME	Indicator	The bus request (BR) VME LED is lit yellow when the local processor requests bus mastership on the VMEbus
		BM VME	Indicator	The bus master (BM) LED is lit when the MCP is the current bus master
		DS VME	Indicator	The data strobe (DS) VME LED is lit whenever the processor has placed a data strobe on the VMEbus
		DS VSB	Indicator	The DS VSB LED is lit whenever the processor has placed a data strobe on the VSB
		1, 2	Switch	The rotary switches are 4—bit hexadecimal encoded; They are completely under software control; normal MDP operation is when the switches are set on position “F”.

Table 3—3. Modulator/Doppler Predictor PWA Controls and Indicators (Continued)

FIG. REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3—2	Modern Control Processor PWA (Continued)	CACHE	Switch	The CACHE switch enables the 68030 onchip data cache with its 256 bytes when in the “down” position; In the “up” position, the onchip cache is deactivated by hardware, overriding all software settings
		R/H	Switch	The RUN/HALT (R/H) switch enables or disables local operation of the CPU and the FPCP; This switch can be used to debug multiprocessor software packages and to disable a CPU board in an application when a failure has occurred but power can’t be switched off; The processor is in the halt state if the switch is in the “up” position; Normal operation is provided when the switch is in the “down” position
3—2	Data Conditioning and Encoding PWA	MCP FAIL	Indicator	Turns on to indicate that the MCP PWA has failed its BIT test
		TIME FAIL	Indicator	Turns on to indicate that the TIME PWA has failed its BIT test
		SYNTH FAIL	Indicator	Turns on to indicate that the SYNTH PWA has failed its BIT test
		DCEC FAIL	Indicator	Turns on to indicate that the DCEC PWA has failed its BIT test
		FMOD FAIL	Indicator	Turns on to indicate that either the FMOD or the GMOD has failed its BIT test
		PS1 FAIL	Indicator	Turns on to indicate that the power supply No. 1 has failed its BIT test
		PS2 FAIL		Turns on to indicate that the power supply No. 2 has failed its BIT test

Table 3—3. Modulator/Doppler Predictor PWA Controls and Indicators (Continued)				
FIG. REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3—2	Data Conditioning and encoding PWA (Continued)	OVER TEMP		Turns on to indicate that the temperature sensor in the MDP is reporting out—of—limits temperature; See paragraphs 3—15.8 and 3—16.3
		PHASE LOCK	Indicator	Turns on to indicate that the phased—lock loop supporting the selected Shuttle S—band mode has locked to the desired frequency
3—2	Synthesizer PWA	LOCK	Indicator	Turns on to indicate that the 61.5—MHz PLL, 140—MHz PLL, and 10—MHz reference input are normal

Table 3—4. Power Supply No. 1 Controls and Indicators				
FIG. REF.	FIGURE MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3—3	V1 (+5V ADJ))	1A2V1	Potentiometer	Used to adjust the +5.0 Vdc output voltage
3—3	V2 (+15V ADJ)	1A2V2	Potentiometer	Used to adjust the +15.0 Vdc output voltage
3—3	V3 (—15V ADJ)	1A2V3	Potentiometer	Used to adjust the —15.0 Vdc output voltage
3—3	V4 (+5 RF ADJ)	1A2V4	Potentiometer	Used to adjust the +5 RF Vdc output voltage
3—3	Over Temp	1A2DS1	Indicator	Turns on to indicate a fan failure

Table 3−5. Power Supply No. 2 Controls				
FIG. REF.	FIGURE MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3−4	V1 OVP	1A3V1A	Potentiometer	Used to adjust the overvoltage protection threshold voltage level for the −5.2 Vdc output voltage
3−4	V1 (−5.2V ADJ)	1A3V1B	Potentiometer	Used to adjust the −5.2 Vdc output voltage
3−4	V2 (+12V ADJ)	1A3V2	Potentiometer	Used to adjust the +12 Vdc output voltage
3−4	V3 (−12V ADJ)	1A3V3	Potentiometer	Used to adjust the −12 Vdc output voltage

TEST indicator is turned on. If any routine does not complete successfully, the FAILURE indicator is turned on and the MDP halts operation and/or sets the applicable LRU fail status. Upon successful completion of the confidence BIT, the TEST indicator is turned off, and the MDP enters the standby state. The routines are as follows:

a. System random access memory (RAM) test.

b. Central processing unit (CPU) test.

c. Kernel initialization.

d. Interrupt initialization

e. MIL−STD−1553 test.

f. I/O initialization.

g. VME test.

h. Environment test.

i. Indicators test.

3−15.1 RAM Test

This test performs four different write, read, and compare operations on the MCP RAM. The RAM test uses a 5's pattern, an A's pattern, an address pattern, and inverse address pattern to determine the RAM health. If any RAM locations fail, the front panel FAULT LED is turned on, the status register is loaded with a RAM fail indication, and processing is halted.

3−15.2 CPU Test

This test performs four different tests on the MC68030 CPU resident on the MCP PWA. The first test verifies operation of the CPU data, address, and control registers. The second test verifies operation of the CPU's instruction set. The third test verifies operation of the CPU addressing modes. The fourth test verifies operation of CPU exception processing, including the following exceptions: bus error, address error, illegal instruction, zero division, check instruction, TRAPV instruction, privilege violation, trace, trace on change, line−A emulation, line−F emulation, format error, and the 16 software traps. If any CPU

test fails, the front panel FAULT LED is turned on, the status register is loaded with a CPU fail indication, and processing is halted.

3–15.3 Kernel Initialization

This function creates the kernel system environment using the values supplied in the kernel configuration table. Once the kernel pointers have been set up, the kernel workspace is set up, the task control blocks are created, the user stacks are set up, the interrupt service routines (ISR) stacks are created, and the internal kernel variables are initialized. If any of the kernel initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start–fail indication, and processing is halted.

3–15.4 Interrupt Initialization

This function initializes the interrupt circuitry to allow hardware interrupts to the MCP. All device–generated interrupt vectors and autovectors are initialized in the exception vector table during this routine. If any of the interrupt initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start–fail indication, and processing is halted.

3–15.5 MIL–STD–1553 Test

This function verifies operation of a DDC bus–61553 MIL–STD–1553 device. Tested features include buffer RAM, device configurability, and data transmission/reception in an internal loopback mode. The buffer RAM test writes, reads, and compares 5's, A's, address, and inverse address test patterns. The device configurability test writes, reads, and compares a configuration test pattern to the registers and then resets the registers and reads their reset value. The loopback test sets up the TIME for 1553 operation, loads test data messages, and instructs the 1553 device to transmit the data. If the data does not transmit correctly or during a specified time, the front panel FAULT LED is turned on, the status register is loaded with a start–fail indication.

3–15.6 I/O Initialization

This function initializes the MIL–STD–1553 remote terminals and RS–232C (RS–232 is not applicable to the MDP) device to a known state and verifies that state. If any of the I/O initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start–fail indication.

3–15.7 VME Test

This function verifies proper operation of the DCEC VME data transfer bus. A test word is written to the DCEC, read back from it, then compared to the expected word. If the words do not compare, the VME bus test fails. If a bus exception occurs during access, the test fails. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed, and status can be determined via the DCEC LED (CR3 – DCEC failure).

3–15.8 Environment Test

This function verifies proper operation of the TIME PWA's A/D converter and proper voltage and temperature levels. The TIME status register is read for proper bit settings. If the WRAM bit is not set, the test fails. With the WRAM bit set, the test reads the TIME digitized voltage values for 5 Vdc, RF 5 Vdc, 12 Vdc, 15 Vdc, and the unit temperature. If any of these environmental parameters are not within their specified normal ranges, the test fails. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed, and status can be determined via the DCEC LEDs (CR5 – PS1 failure, CR6 – PS2 failure, and CR7 – temperature overrange).

3–15.9 Indicators Test

This function verifies proper indicator operation by turning all indicators on for one second. Verification of proper operation is by visual inspection of the indicators while they are turned on.

3–16 Online Bit

Online BIT is a function of the schedule 1–second tasks. Online BIT is run as a continuous process,

once per second, during all active MDP states. The routines are as follows:

a. Monitor GMOD.

b. Monitor exceptions.

c. Monitor time.

d. Monitor environment.

e. Monitor synthesizer lock.

f. Monitor 1 PPS.

g. Monitor automatic level control levels.

3−16.1 Monitor Exceptions

This function continually monitors any unexpected CPU exceptions that would set an MCP LRU failure, RS−232 channel 1 or 2 error status/spurious interrupt that would set an MCP LRU failure (not applicable to MDP), and the 1553 channel 1 error status/spurious interrupt that would set a TIME LRU failure. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the DCEC LEDs (CR0 − MCP failure and CR1 − TIME failure).

3−16.2 Monitor Time

This function monitors the 1−second, 100−millisecond, 10−millisecond, and 1−millisecond interrupts and compares them to relative nominal values. If this value varies by more than one count, the TIME LRU is flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome, and status can be determined via the DCEC LED (CR1 − TIME failure).

3−16.3 Monitor Environment

This function verifies proper operation of the TIME PWA's A/D converter and proper voltage and temperature levels. The TIME status register is read for proper bit settings. If the WRAM bit is not set, the test fails. With the WRAM bit set, the test reads the TIME digitized voltage values for 5 Vdc, RF 5 Vdc, 12 Vdc, 15 Vdc, and the unit temperature. If any of these environmental parameters are not within their specified normal ranges, the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the DCEC LEDs (CR1 − TIME failure, CR5 − PS1 failure, CR6 − PS2 failure, and CR7 − temperature overrange).

3−16.4 Monitor Synthesizer Lock

This function checks the reference 10−MHz bit for assertion and either of the 140−MHz or 61.5−MHz bits for nonassertion. Any of these conditions causes the SYNTH LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome, and status can be determined via the DCEC LED (CR2 − SYNTH failure).

3−16.5 Monitor 1 PPS

This function samples the Synchronization Complete bit and the Synchronization Error bit for a true setting. This condition causes the TIME LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome, and status can be determined via the DCEC LED (CR1 − TIME failure).

3−16.6 Monitor ALC Levels

This function monitors the ALC signal levels to detect a modulator (FMOD or GMOD) LRU failure. The ALC signal levels are digitized via the TIME ADCs and compared with nominal values. Any level not within the specified range causes the FMOD or GMOD LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the DCEC LED (CR4 − FMOD failure).

3−17 Extended Bit

The extended BIT is executed only upon command via the 1553 interface (remote control) or front panel (local control). While extended BIT is in progress, all other MDP functions, except those which maintain time, are paused. Upon completion of extended BIT, the unit returns to the

standby state. The extended BIT routines are broken up into two groups; group 1 is a basic functions test and group 2 is a modulator functions test. The modulator functions test routine is the DCEC test. The basic functions test routines are as follows:

a. MCP test.

b. VME test.

c. TIME test.

3—17.1 MCP Test

3—17.1.1 The MCP test passes if both subtests pass; the 68030 subtest and programmable interval timer (PIT) subtest. The 68030 subtest performs four different tests on the MC68030 CPU. The first test verifies the operation of the CPU data, address, and control registers. The second test verifies operation of the CPU's instruction set. The third test verifies operation of the CPU addressing modes. The fourth test verifies operation of CPU exception processing.

3—17.1.2 The second subtest verifies operation of the two MCP PITs. This subtest tests the PIT's registers, timers, and interrupts. The registers are tested by writing and reading a test word to/from each register and verifying that the word read from the register is the same as the word written to the register. The two PIT timers are tested by comparing their measurement of a short period of time. This subtest fails if a register data write/read is inconsistent or if the PIT timers do not measure a period of time within +/— 5% of each other or if the PIT interrupts do not occur. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome, and status can be determined via the DCEC LED (CR0 — MCP failure).

3—17.2 VME Test

The VME test verifies operation of the VME data transfer bus. A test data word is written to and/or read from each the VME slave LRUs (TIME and DCEC). If a bus exception occurs during LRU access, this test fails. On those LRUs that have a write/read capability, a test word is written to the LRU and then compared to the test word read from that LRU. If the test data words do not compare, this VME bus test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 2) can be determined via the DCEC LEDs (CR1 — TIME failure and CR3 — DCEC failure).

3—17.3 TIME Test

The TIME test performs two independent tests on the TIME PWA. The first test verifies that the four timing interrupts (1, 20, 100, and 1000 pps) occur within a specified tolerance. The second test verifies that the 5—Vdc reference signal is within a specified tolerance. The intervals of the timing interrupts are measured by a PIT counter and the 5—Vdc reference input to the TIME A/D converter is converted to a digital representation and verified. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome, and status can be determined via the DCEC LED (CR1 — TIME failure).

3—17.4 DCEC Test

The DCEC test configures the DCEC for a signature test. The modulated output data from the signature test is compared with expected values and also the DCEC status is verified. The test passes if the DCEC status and signature test results are as expected. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome, and status can be determined via the DCEC LED (CR3 — DCEC failure).

Section 4 — Theory Of Operation

4−1 Introduction

This section provides a functional description of the Modulator/Doppler Predictor (MDP). A general functional description is presented at the block diagram level, followed by individual detailed descriptions of the unit's major functions and hardware/firmware components. The detailed descriptions are supported by timing, flow, logic, and schematic diagrams, when necessary. The information contained in this section is keyed to the Level 1 maintenance procedures in section 5.

4−2 Detailed Functional Description

The MDP processes all SSA, MA, KSA low data rate forward service data and KSA high data rate forward service data for the STGT USS TDRSS. Having the capability of supporting each of these configurations, the MDP can be used interchangeably in any of the unique equipment groups. Although the MDP supports these configurations, not all of the MDP's functional capabilities are required for each. Refer to figure 4−1 for the following functional descriptions.

4−3 Firmware Descriptions

The MDP contains two distinct firmware programs, the executive program (Exec) and the MDP program. The MDP is an application program that provides the necessary scheduling and control of the MDP during operations. The executive program provides I/O services for the MDP application program.

4−3.1 Executive Program

The Exec provides the application program with a real−time operating system. The operating system provides multitasking and resource management of unit input/output. Part of the Exec consists of the VRTX32 multitasking kernel that provides the multitasking scheduling and memory resource management functions. The Exec is made up of the following function design units (FDUs) and together combine to provide an integrated interface between the hardware and the application program:

a. Power−On and Exec Initialization. This FDU is started by either a hardware reset or an application call execute command (Excmd) to reinitialize. When this occurs, this FDU checks the system RAM, boots all code into the system RAM, and then starts operation from system RAM. The system kernel is initialized, the event vector table is set up, and I/O devices are initialized. Finally, the I/O devices are tested as part of the online BIT FDU, and the application program is started.

b. Input/output. I/O FDUs (RS−232 and MIL−STD−1553) typically have two entry points that consist of functions that the applications call (i.e., Exec Read and Exec Write) and interrupt service routines (ISRs) that are invoked by the hardware−generated interrupts. The application program uses the I/O FDUs to interface to the system I/O hardware.

c. Event Handlers. This FDU provides the interrupt service routines for the signal processing and timing hardware interrupts that schedule the time−critical signal processing.

d. Exception Handlers. This FDU interfaces the MC68030 to error processing and recovery ISRs. These ISRs also allow for report generation that details the error that was encountered.

e. Download Code. This FDU provides the capability of downloading software code to the MCP processor. Ephemeris data download is also included in this FDU. The download is via the MIL−STD−1553 bus.

f. Exec BIT. This FDU provides confidence tests for the I/O devices that can be called by the power−on and Exec initialization FDU or by the application program.

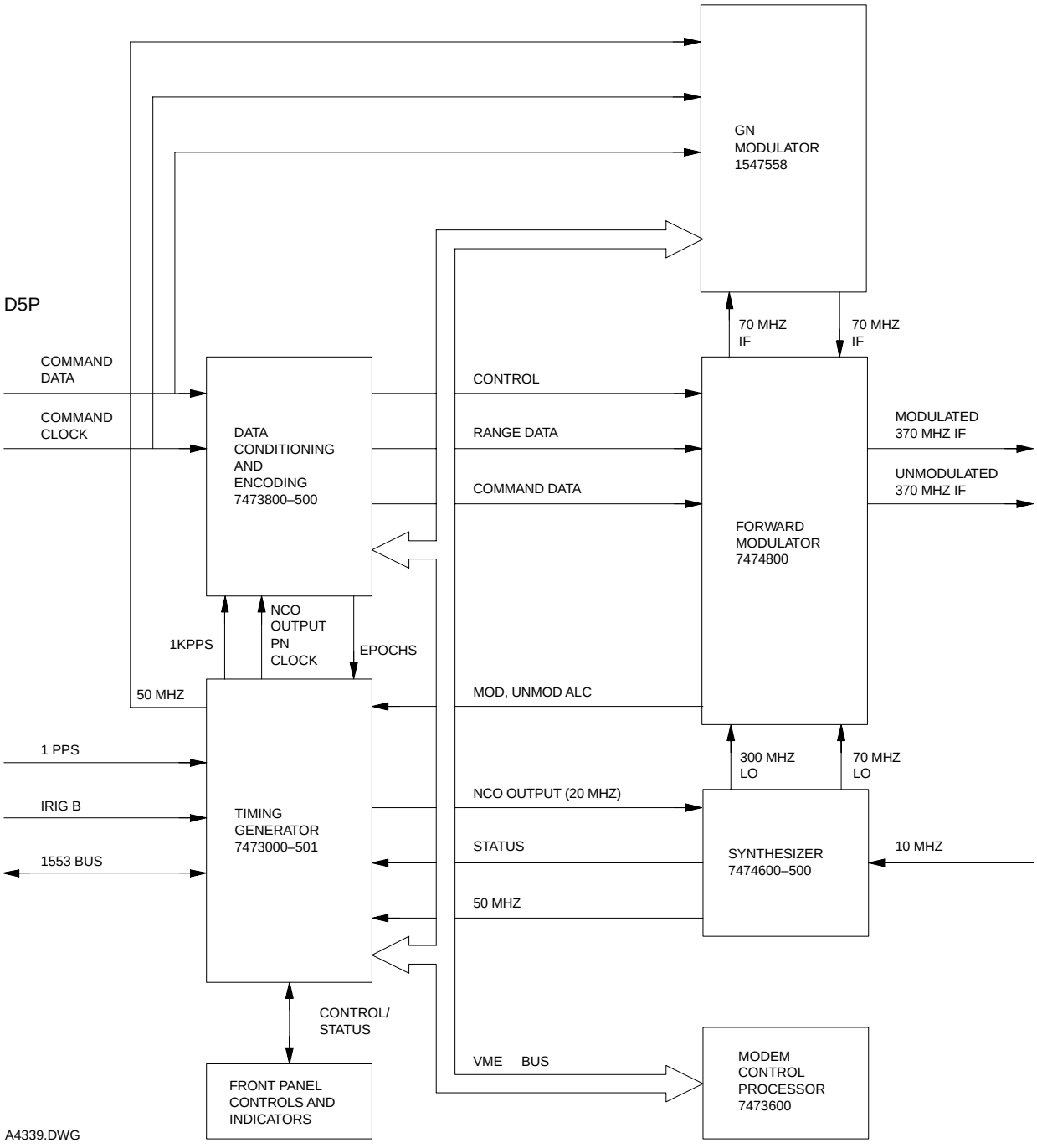


Figure 4—1. Modulator/Doppler Predictor Functional Block Diagram

4−3.2 MDP Program

The MDP program is the master application program of the MDP. The MDP program's purpose is to control modulation and Doppler compensation on the forward service signal. It also provides status updates to the ADPE via the MIL−STD−1553 bus interface. The MDP is remotely controlled via the 1553 interface. The MCP program also interfaces with the TIME and DCEC PWAs. The MCP program is made up of the following functions:

a. Command Processor Function. The command processor function processes the commands received over the 1553 bus from the ADPE. Commands over the 1553 bus are received asynchronously, and this function processes each command upon receipt. Some commands contain an effective time which determines when the action defined within the command is to take place. On startup, this function clears the 1553 interface, initiates input from the 1553 bus, and processes that input. Verification is made that the LOCAL/REMOTE switch is in the REMOTE position before processing any commands. When applicable, the ephemeris database is updated. This function is capable of filling the ephemeris database to its maximum size of 50 minutes with a limit of 10 minutes of ephemeris data per transfer.

b. Time Management Function. This function maintains time−of−year (TOY) and the forward epoch timer that are used throughout the application firmware. The TOY, maintained by the Time PWA, is updated once a second with a resolution of 1 millisecond. This function maintains 1−, 10−, and 100−millisecond counters. If, while in standby state, TIME is not in sync, a re−sync command is issued. The update epoch measurement reads the first epoch measurement following the 1−PPS interrupt event. The epoch event is masked on prior to the 1−PPS interrupt and masked off after the epoch measurement is read.

c. Performance Monitor Function. This function consists of the online BIT, extended BIT, confidence BIT, manage fault light, and prepare status reports. Refer to section 3 for explanations of BITs and manage fault light functions. The prepare status reports function examines status and data from all major data sources and converts the information into the appropriate status report format. All reports are available to be read by the 1553 bus interface at the 300−millisecond mark after each 1−PPS. The reports consist of the following: configuration report, performance report, extended BIT report, and time transfer report.

d. Forward Modulation Controller Function. This function controls the forward services signal modulation. Configuring the DCEC/FMOD/GMOD hardware is enabled when the command processor function receives a configuration command. The hardware is configured to generate the long and short codes. Table 4−1 shows the PN configurations used by the MDP. The range channel code generator uses the feedback taps, and the command channel code generator and the S−Shuttle code generator use the register A initial condition to generate all short code iterations. The PN generators are then loaded with a code state value of zero so that the master PN epoch occurs at the service start time. The DCEC/FMOD status and supply information is read by the performance monitor function for output to the ADPE.

e. Ephemeris Processing/Carrier Sweep Function. This function is made up of the following subfunctions: Doppler compensation, frequency sweeping, and numerically controlled oscillator (NCO) controller. The Doppler compensation function provides both IF carrier and PN chip rate Doppler compensation. It follows the commanded PN and IF frequency−time profile provided in the ephemeris. IF carrier compensation and PN chip rate compensation are also independently compensated on command from the ADPE. This function generates the Doppler PN code and carrier frequency every 2 milliseconds. For IF Doppler compensation, the maximum step for IF deviation is 0.8 Hz from

Table 4—1. PN Configurations

P/N NAME	PN SPREAD (1)	PN LENGTH	PN RATE	PN FAMILY	TIME TRANSFER
KSA Range Channel	Yes	261888	Approx. 3 Mcps	18—stage shift register (feedback taps)	Yes (1st epoch)
KSA Command Channel	Yes	2047	Synchronous to range channel	Short code (use register A initial value)	No
KSH Command Channel	Yes	2047	Approx. 3 Mcps	Short code (use register A initial value)	No
SSA Range Channel	Yes	261888	Approx. 3 Mcps	18—stage shift register (feedback taps)	Yes (1st epoch)
SSA Command Channel	Yes	2047	Synchronous to range channel	Short code (use register A initial value)	No
SSH Command Channel	Yes (2)	1023	11.232 Mcps	S—band Shuttle (use register A initial value)	No
MA Range Channel	Yes	261888	Approx. 3 Mcps	18—stage shift register (feedback taps)	Yes (1st epoch)
MA Command Channel	Yes	2047	Synchronous to range channel	Short code (use register A initial value)	No

NOTES: (1) No PN in channel if commanded.
(2) Carrier Doppler and PN Doppler are synchronously related except for SSH.

the previous time increment. For PN Doppler compensation, the maximum step for PN deviation is 0.004 chips/second from the previous time increment. The frequency sweep function initiates linear frequency sweeping of the carrier and PN when commanded by the ADPE. Frequency sweeping is in addition to the Doppler compensation profile and occurs for 120 seconds. For times beyond 120 seconds, the modified profile consists of the original profile plus 3.094 kHz for SSA and MA or plus 30.8490 kHz for KSA.

The PN rate is swept synchronously with the carrier at a PN rate to carrier frequency ratio of 31/(240 x 96) for SSA and 31/(1496 x 96) for KSA. The NCO controller function updates the PN code and carrier NCOs independently every 2 milliseconds. This function adds forward translation frequency and the IF frequency to the values from the Doppler compensation function and the frequency sweep function and scales it to fit into the NCO register before updating the NCOs.

4−4 States Of Operation

4−4.1 The MDP operating states consist of six major Forward operating states. During operation, the Integrated Receiver (IR) uses MDP parameters and commands for coherent service tracking. The IR is a unit within the return service (downlink) equipment. The parameters used by the IR are: IF offset frequency, translation frequency, PN modulation configuration, and the Doppler configuration. Refer to figure 4−2 for the following explanation of the six MDP operating states.

4−4.2 The confidence test in progress state is entered at powerup or reset and the TEST LED is turned on. During this state, the MDP executes its confidence test and does not respond to any 1553 bus communications. This state completes in less than 10 seconds, and the TEST LED is turned off. If the confidence test fails, the FAULT LED is turned on and remains on.

4−4.3 The standby state indicates that the MDP is ready to receive a configuration command. Upon receipt of both a common configuration command and a specific configuration command, the MDP starts configuration of the unit. The specific configuration command contains configuration parameters that are specific to the MDP (not common or synchronous to the IR or PTE). The common configuration command contains configuration parameters that are common and require time synchronization with the IR.

4−4.4 The extended BIT state is entered by an extended BIT command over the 1553 bus (remote) or front panel display (local) and exits upon completion or by termination of BIT by either the front panel or a 1553 bus command. The configuration in progress state indicates that the MDP is dedicated to the configuration of the unit. No other signal modulation or control is done while in this state.

4−4.5 The MDP is configured in accordance with the specific and common configuration commands received via the 1553 bus interface. Upon completion of the configuration, the unit transitions to the configured state. The configured state indicates that the MDP has completed all unit configuration processes and is ready to accept the start service command. Upon acceptance of a start service command, the MDP enters the in service state and signal modulation and processing begins.

4−5 MDP Configurations

The MDP supports four unique configurations for STGT USS forward services (see figures 4−3, 4−4, 4−5, and 4−5−a). The MDP continuously monitors the user data/clock signals input and periodically provides data/clock presence information to the ADPE via the 1553 bus interface. Rate 1/3 convolutional encoding and NRZ to biphase conversion are provided to support S−band Shuttle services. The MDP supports both spread and nonspread PSK modes and supports spreading with both long and short codes. For PSK modes, the range and command channels are QPSK modulated and frequency upconverted to either 369.5 MHz for SSA modes, 370.0 MHz for KSA modes, and 371.40 MHz for MA modes (see table 4−2 for a breakdown of the MDP carrier tuning ranges). The MDP also supports BPSK operation for highrate modes and when PN spreading is disabled. The MDP also supports the following PM modes: Sinewave Subcarrier, Squarewave Subcarrier, and Direct Phase Modulation (PM/PCM). When the input data clock, received from the control HWCI, is clamped to a logic 1 state, the MDP inhibits any input data from modulating the carrier.

4−6 Carrier/Code Compensation

4−6.1 All configurations provide compensation for Doppler so that the carrier and code arrive at the user spacecraft receiving system within a predictable tolerance. This feature minimizes the Doppler resolution requirements of the user spacecraft receiver and is continuously available to facilitate reacquisition by the user spacecraft in the event of loss of lock of the TDRSS forward service signal. Doppler compensation is inhibited via command by user.

4−6.2 The MDP provides the capability to independently provide carrier and PN forward service Doppler compensation in SSHF mode. The MDP sets the code generator, code NCO, and carrier NCO to the initial state prior to generating the forward signals.

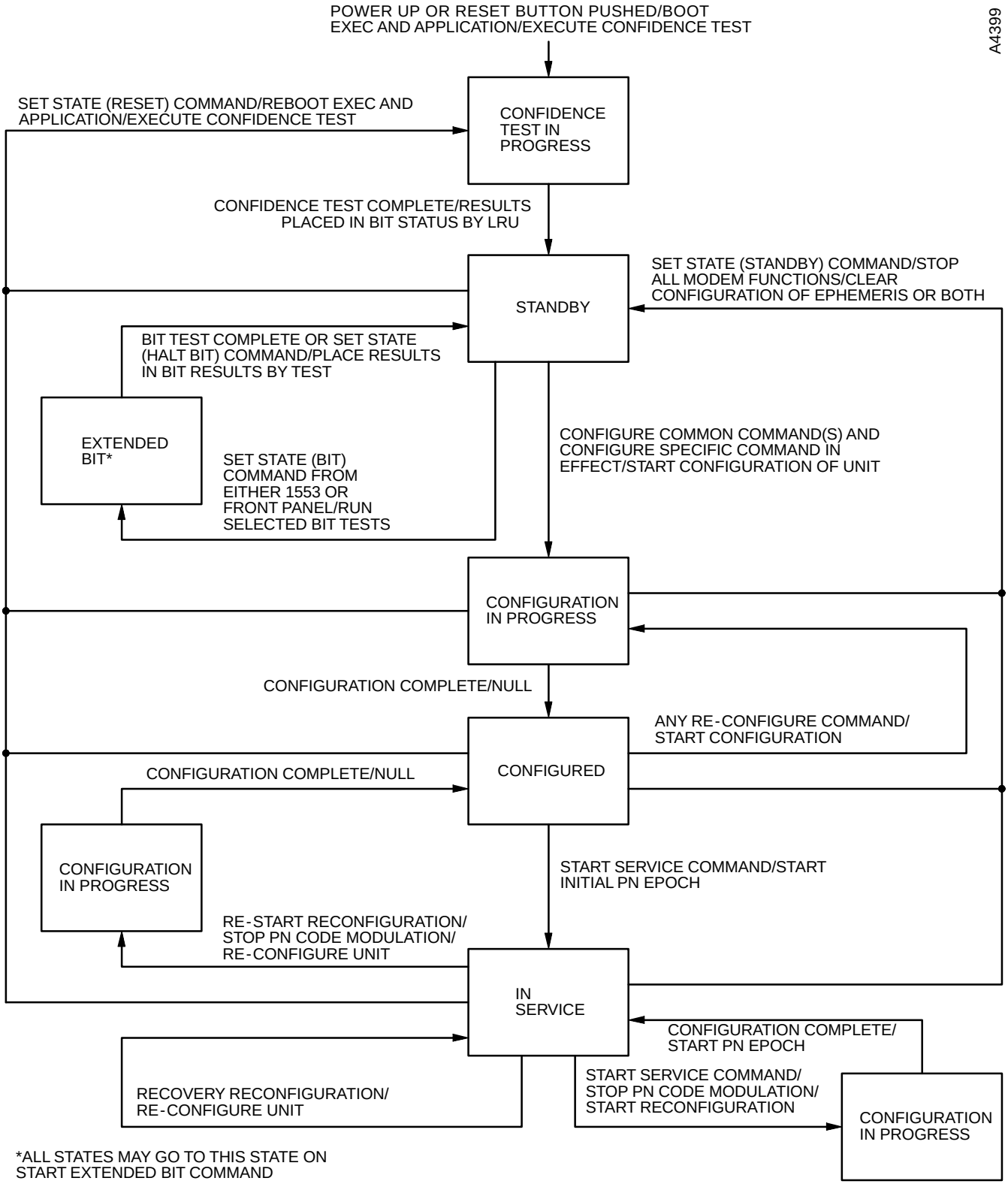


Figure 4—2. MDP Operating States

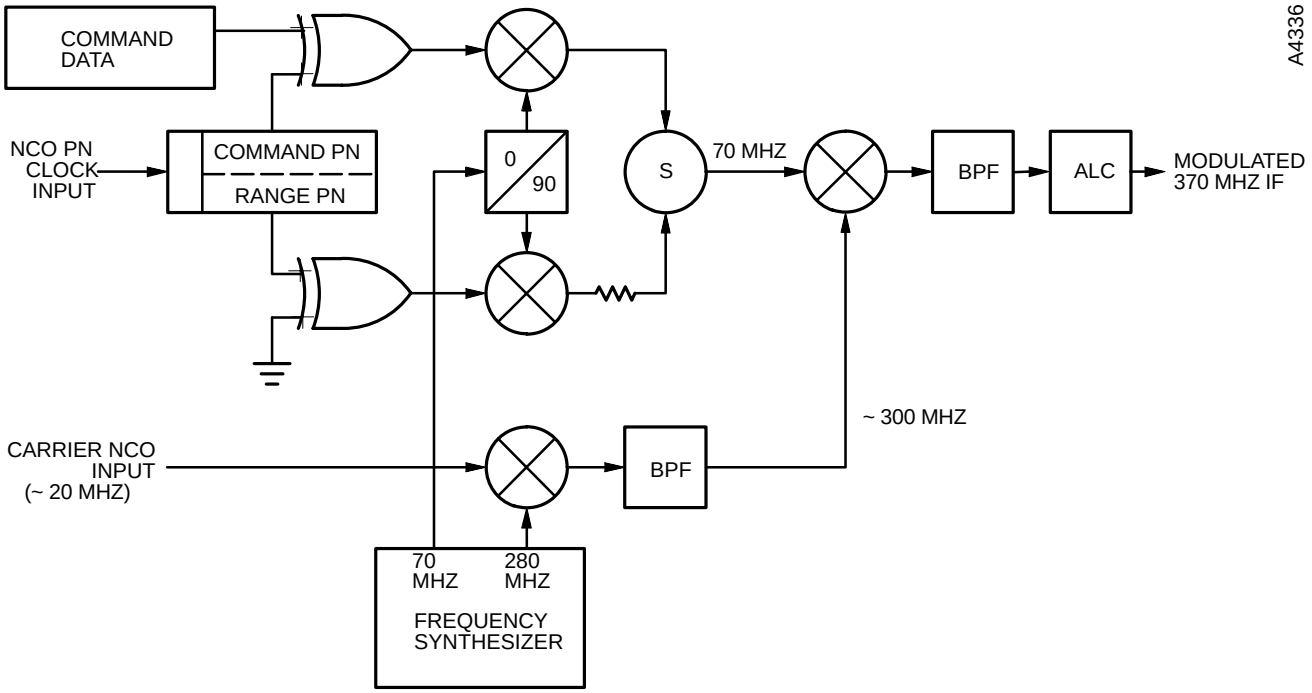


Figure 4—3. Modulation Configuration Used for Non—Shuttle MA, SSA, and KSA Bit Rates Less Than or Equal to 300 Kbps

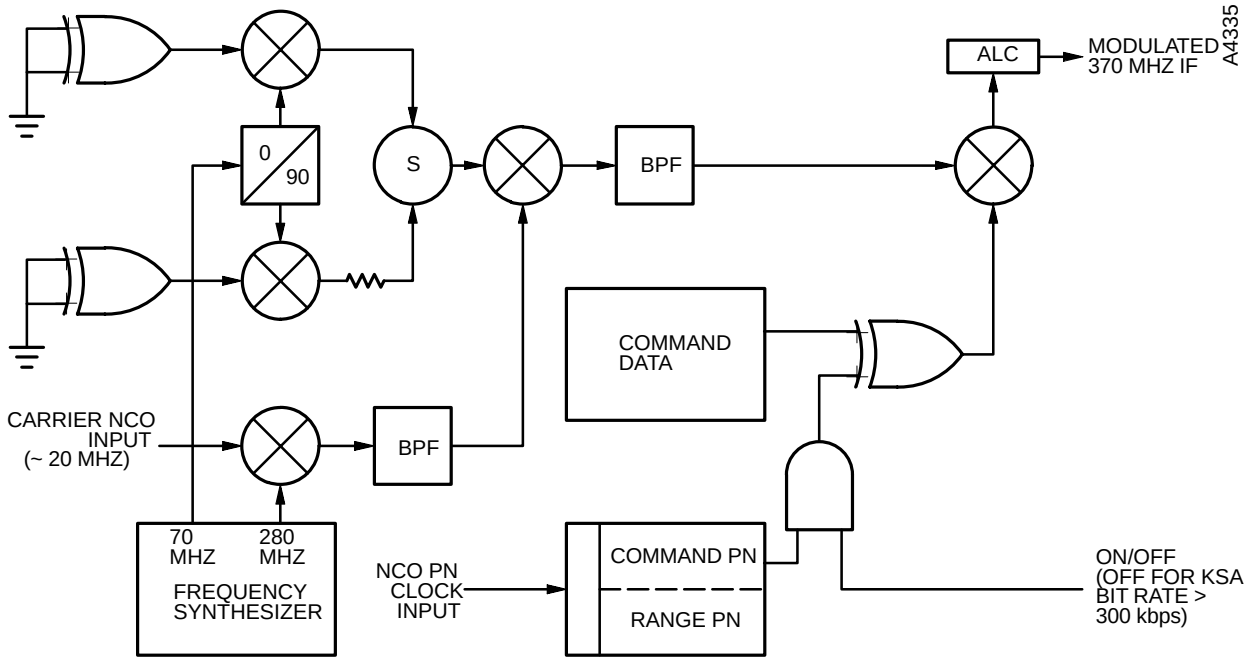


Figure 4—4. Modulation Configuration Used for Shuttle K—Band and KSA Bit Rates Greater Than 300 Kbps

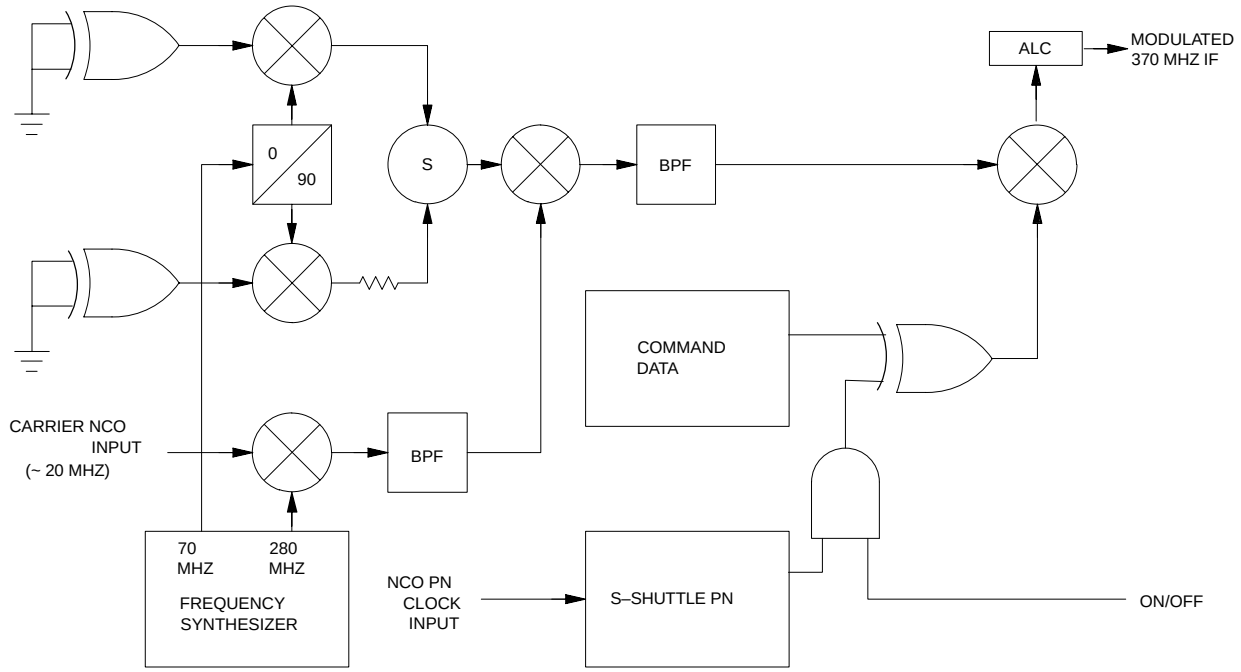


Figure 4—5. Modulation Configuration Used for Shuttle S—Band

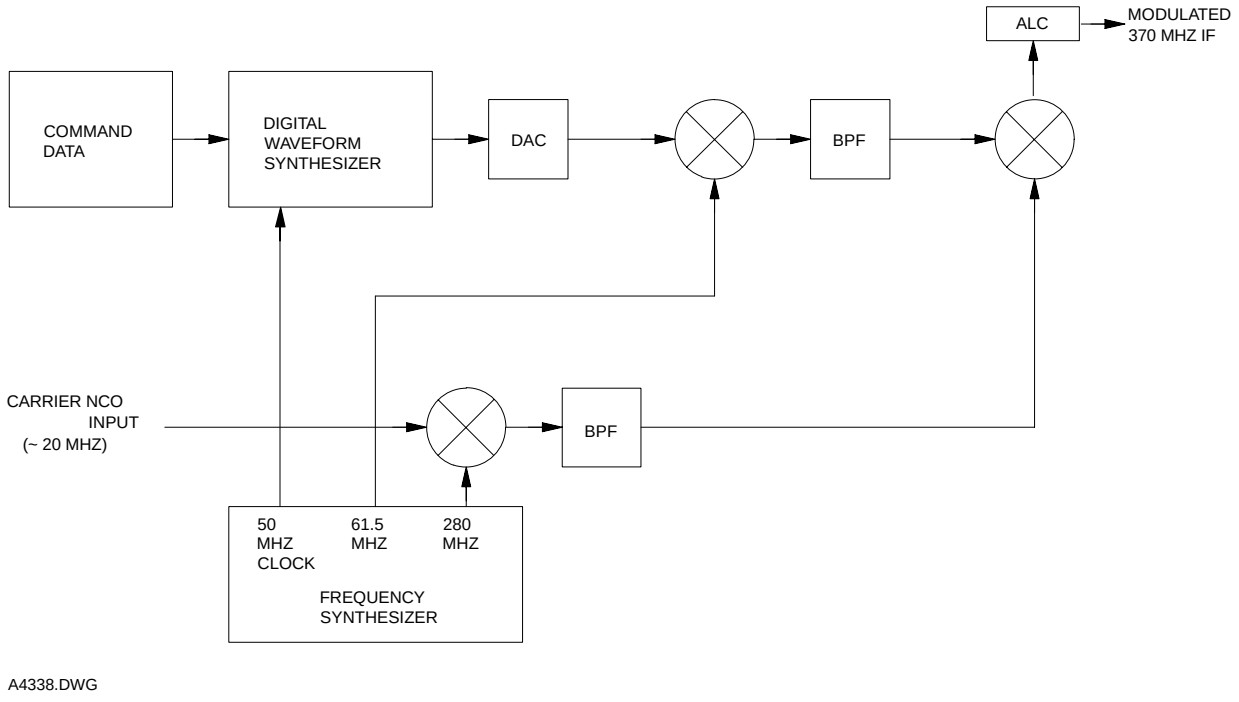


Figure 4—5—a. Modulation Configuration Used for Subcarrier and Direct Phase Modulation

Table 4−2. MDP Carrier Tuning Ranges			
PARAMETER	SSA	KSA	MA
Referenced center	369.500 MHz	370.000 MHz	371.400 MHz
User tuned offset frequency	+/−0.250 MHz	+/−0.700 MHz	+/−0.100 MHz
Forward Doppler range	+/−0.085 MHz	+/−0.560 MHz	+/−0.085 MHz
Forward sweep range	+/−3094 Hz	+/−30849 Hz	+/−3094 Hz
Total tuning range	369.50 +/−0.338094 MHz	370.00 +/−1.290849 MHz	371.400 +/−0.188094 MHz

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4—6.3 Ephemeris processing maintains an ephemeris database with a maximum size of 50 minutes' worth of data. The MDP is capable of saving ephemeris updates up to 60 minutes past its current time. Any ephemeris data greater than 60 minutes in the future is discarded. Ephemeris data provides for compensation of the carrier and code.

4—7 Carrier Sweep and Break Lock

4—7.1 Carrier sweep is used to assist in forward user acquisition if the user state vector is suspect (i.e. near or greater than +/—9 seconds off in time for S—band or +/—4.5 seconds for K—band) or the transponder receiver "best lock" frequency is suspect (i.e. temperature drift considerations).

a. When configured for "SN Sweep" by the databus, carrier sweep operates as follows: When carrier sweep is commanded, the MDP modifies the commanded Doppler profile by adding to it a linear ramp having a starting value of —3.0940 kHz for SSA and MA and —30.8490 kHz for KSA at the specified execution time. The final value of the ramp is +3.0940 kHz for SSA and MA and +30.8490 kHz for KSA; 120 seconds after the commanded execution time. In the event of subsequent sweep commands, the sweep ramp is always applied to the commanded Doppler profile. For times beyond the completed sweep, the modified Doppler profile is equal to the commanded Doppler profile plus the final value of +3.0940 kHz or +30.8490 kHz.

b. When configured for "GN Sweep" by the databus, the MDP modifies the output frequency profile by adding the GN sweep profile to the Doppler profile that is in effect at the time. A single GN sweep is made up of four sweep segments, each segment lasting "GN Sweep Duration," in seconds. The four segments are: (1) from the nominal Doppler profile down to "GN Sweep Range" (Hz) below the Doppler profile frequency, (2) from that frequency back to the nominal profile frequency, (3) from the nominal frequency up to "GN Sweep Range" above the nominal Doppler profile frequency, and (4) from that frequency back down to the nominal profile frequency. If the sweep count command parameter is a positive integer, the MDP will execute this number of complete sweeps contiguously, ending at the Doppler profile frequency and following the profile. If the sweep count parameter is zero, the MDP will repeat this sweep pattern until another sweep command is received. The MDP will discontinue the sweep on the first return to the Doppler profile following the second sweep command.

4—7.2 The break lock function is used to break lock on the forward link when it is suspected that the user transponder has false locked. Break lock command causes the MDP to initiate an abrupt change in output frequency, where the step size and direction are provided as a command parameter. The step size in 1 kHz increments can be between +/—335 kHz for SSA, +/—1.260 MHz for KSA, and +/—185 kHz for MA.

4—8 Command and Range PN Channels

4—8.1 All MA, SSA, and KSA configurations with a data rate less than or equal to 300 kbps include separate but simultaneous command and range channels. All Shuttle configurations and KSA configurations with a data bit rate greater than 300 kbps inhibits command and range channels. The command and range channels provide a solution to the conflicting requirements for range ambiguity resolution and multipath protection. The command channel (applied to the I channel of the modulator) includes a rapidly acquirable PN code and contains the forward service data.

4—8.2 The range channel (applied to the Q channel of the modulator) is acquired separately and contains a PN code that satisfies the range ambiguity resolution requirements. For Shuttle S—band and K—band configurations, there is no data channel ambiguity to be resolved since there is only a single data channel. For the Shuttle S—band, data phase ambiguity is resolved on the Shuttle by rate 1/3 Viterbi decoding. For the Shuttle K—band, the data phase ambiguity is resolved on the Shuttle by frame synchronization.

4—8.3 Prior to transmission, the epoch (the all 1's condition) of the range channel PN code is time synchronized to one of the periodic epochs of the command channel PN code generator. Because user spacecraft command channel acquisition must precede user spacecraft range channel acquisition, this feature limits the range channel PN code search to only 256 chip positions, while the range channel PN code itself contains 261,888 chips. This also permits rapid detection of time spread on the received range channel signal identifying acquisition of a diffuse multipath signal. By the user spacecraft transferring the PN code tracking loop to the range channel after range channel acquisition, subsequent multipath interference is prevented.

4−8.4 PN modulation can be commanded on and off. When PN is on, the carrier is QPSK modulated. When PN is not on, the carrier is BPSK modulated. The exception is Shuttle S−band configuration, which is always BPSK modulated, whether PN modulation is required or not.

4−8.5 Except for Range Zero Set, the MDP always synchronizes the range channel PN code such that its epoch is aligned to within ±25 nanoseconds of the CTFS 1 PPS mark corresponding to the Effective Time of the MDP Start Service Command. For Range Zero Set, the code used on the I channel shall be synchronized such that its epoch is aligned to within ±25 nanoseconds of the CTFS 1 PPS mark corresponding to the Effective Time of the MDP Start Service Command. PN codes used for S−Shuttle and K−Shuttle forward services do not require epoch synchronization.

4−9 Data Input Processing

The MDP provides data formatting, symbol formatting, and encoding of forward user data, as specified. The MDP accepts data rates ranging from 100 bps to 25 Mbps, in increments of 1 bps, within the limits specified for SSA, SSH, KSA, KSH, and MA forward services.

4−9.1 SSA Forward Service (SSAF)

4−9.1.1 For PSK modes, SSAF data rates range from 100 bps to 300 kbps with PN modulation enabled, up to 7 Mbps with PN modulation disabled. The input data format is NRZ−L, −M, or−S. For PSK modes, the MDP accommodates any change to the actual input data rate in this range without being notified by the data bus. No data formatting or encoding is required for SSAF PSK modes.

4−9.1.2 For PM modes, SSAF data rates range from 125 bps to 1 Mps. The input data format is NRZ−L. The input data rate must be consistent with the configuration of the MDP, as configured by the data bus. The MDP can convert NRZ−L data to NRZ−M, NRZ−S, biphase−L, biphase−M, or biphase−S.

4−9.2 SSH Forward Service (SSHF)

SSHF data rates are restricted to 32 kbps for Mode 1 and 72 kbps for Mode 2. The input data format is always NRZ−L. The MDP must be commanded by the data bus to configure for Mode 1 or Mode 2. The input NRZ−L data is convolutionally encoded by the MDP. The encoded symbols are then format converted to Biphase−L by the unit.

4−9.2.1 Convolutional encoding −The encoder for S−Shuttle input data possesses the following characteristics:

a.	Code rate:	1/3
b.	Constraint length:	k = 7
c.	Generator functions:	G1 = 1111001 G2 = 1011011 G3 = 1100101

4−9.2.2 Synchronization − The S−Shuttle encoder synchronizes within 1000 symbols of being configured, or reconfigured, by the data bus provided the correct Mode 1 or Mode 2 input is also configured. Input data rate is to the accuracy of the CTFS.

4−9.2.3 Status Reporting − Encoder synchronization, i.e., encoder lock status, is provided in the MDP Performance Report. Lock status is sampled once per second.

4−9.3 KSA Forward Service (KSAF)

KSAF data rates change from 1 kbps to 25 Mbps. The input data format is NRZ−L, −M, or −S. For data rates less than or equal to 300 kbps, the MDP accommodates any change to the actual data rate without being notified by the data bus. No data formatting or encoding is required for KSAF.

4−9.4 KSH Forward Service (KSHF)

KSHF data rates are restricted to 216 kbps for Mode 1 and 72 kbps for Mode 2. The input data format is NRZ−L only. The data bus informs the unit as to Mode 1 or Mode 2 configuration. The MDP converts the NRZ−L input data to Biphase−L format. No encoding is required.

4−9.5 MA Forward Service (MAF)

MAF data rates range from 100 bps to 10 kbps. The input data format is NRZ−L, −M, or −S. The MDP accommodates any change to the actual input data rate in this range without being notified by the data bus. No data formatting or encoding is required for MAF.

4−10 Modem Control Processor PWA

Refer to figure 4−6 for the following MCP functional description. MCP consists of a 25−MHz 68030 processor based VME bus controller, 1 Mbyte zero−wait state static RAM, four EPROM sockets (271024 EPROMs = 512 bytes), two serial channels (68561 based) − up to 38.4 baud (RS−232 compatible, one channel selectable RS−232/RS−422/ RS−485), and two 24−bit timers. The MCP address select enables the control logic section of the slave boards on the VMEbus by matching address lines A23−A19 with the board select bits of the P2 connector. The remaining 18 address lines (A18−A01) are then used by the control logic to determine the transfer function to be processed.

4−10.168030 Microprocessor

4−10.1.1 The 68030 contains sixteen 32−bit general−purpose address and data registers, two 32−bit supervisor pointers, and one user stack pointer. The non−multiplexed address and data bus can be used in an asynchronous mode to allow optimized hardware interfacing to the buses. Synchronous bus cycles are also supported by the 68030 to accelerate transfers. To offer high data throughput in conjunction to the static RAM, a 16−MHz CPU clock frequency is provided. The 256−byte on−chip data and instruction caches provide a maximum computing rate of 8 MIPS by unloading the system buses from opcode/program fetches.

4.10.1.2 The data bus interface of the 68030 is very flexible and provides a dynamic bus sizing where the data bus size can be adapted. This feature allows the interfacing of 8−, 16−, or 32−bit organized memory and/or I/O devices. For easy exception handling and recover of bus errors, the 68030 stores all internal states in the stack. The MCP contains a local bus interface (LBI). The following devices are connected to the LBI: local SRAM, EPROM, serial I/O controllers (2), parallel interface and timers chips (2), and local interrupt handler chips (2).

4−10.2EPROM and SRAM

The first two read cycles after a reset of the 68030 processor are fetches of the initial interrupt stack pointer and the initial program counter. These cycles are executed under addresses $0 and $4, respectively. A special control logic maps the EPROM down to this address to start the CPU out of the installed EPROMs. The EPROM area is 32 bits wide, offering maximum throughput for the programs running in the EPROMs (SP7472300−XXX). The local SRAM has a memory capacity of 1 Mbyte. The memory module used allows zero wait−state access at the 16−MHz processor clock frequency. The memory is organized 32 bits wide and supports all access modes of the 68030.

4−10.3Serial I/O Interfaces

The MCP contains two RS−232 serial I/O interfaces (not used in the MDP) built around the multiprotocol communications controller (MPCC). The serial interfaces are connected to two 9−pin D−sub connectors on the front panel (not applicable to MDP). One of the two serial interfaces can be reconfigured for RS−422/RS−485 compatibility. Each MPCC interfaces a single serial communication channel using synchronous or asynchronous protocol. In addition to data transfer between the CPU and MPCC, control and status are provided through the 22 directly addressable registers. The on−chip oscillator drives the internal baud rate generator which with two selectable prescalers and a 16−bit divider provides baud rates from 110 to 38400 baud.

4−10.4MPCC Interrupt Handling

Two bus interrupter modules (BIMs) are used to handle all local interrupts. Each MPCC is able to force an interrupt on three different conditions: receiver contains a character, the hardware interface has detected an interrupt generation state, or transmitter is empty. The three different groups of interrupt generation are under software control through some of the 22 registers of the MPCC. The BIM provides a flexible interrupt structure because the interrupt level and the interrupt vector are software−programmable. This allows the adapta-

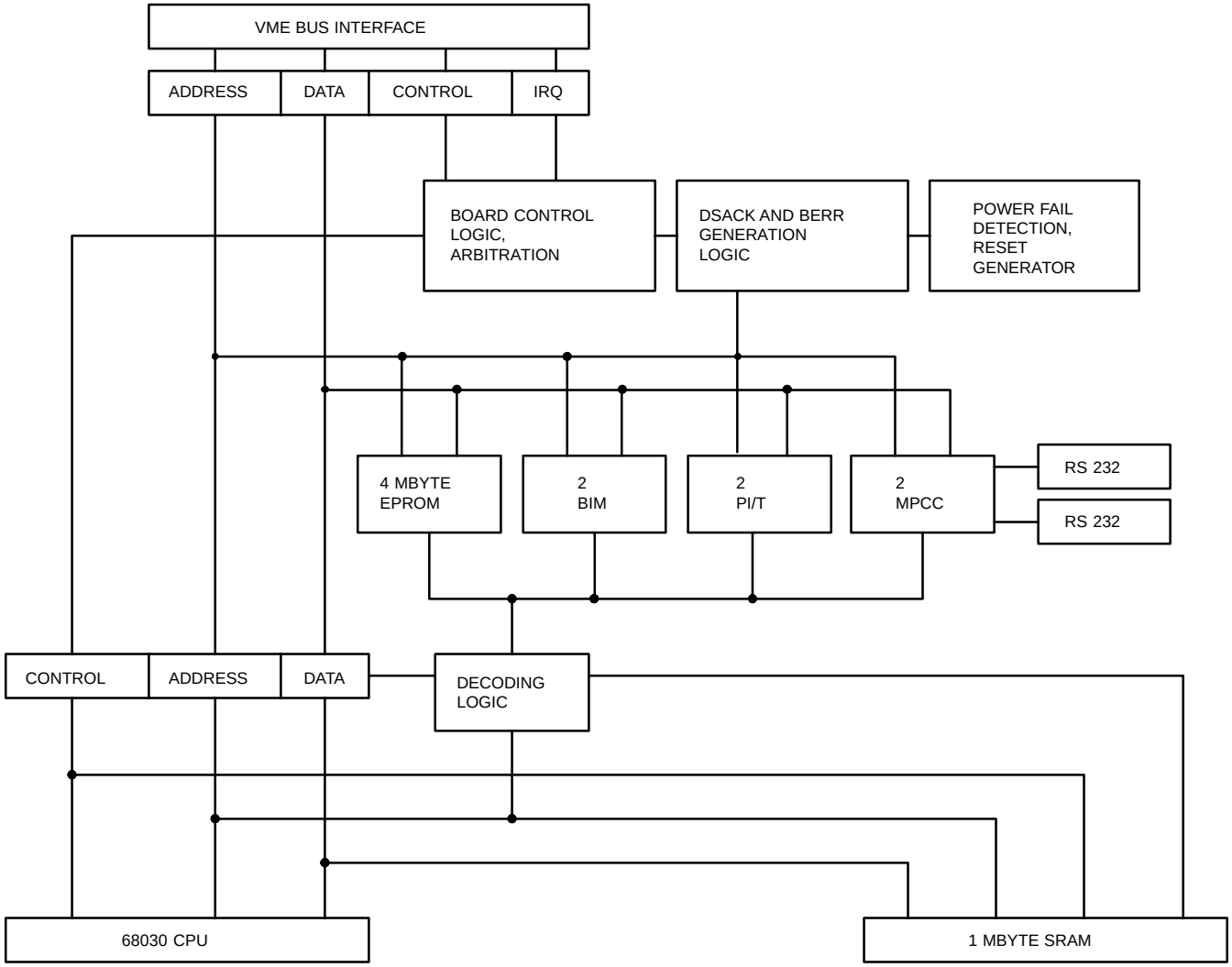

Figure 4—6. MCP Functional Block Diagram

tion of the RS—232 interface on the main board to a wide variety of applications. The two parallel interface and timer (PI/T) devices are used for local control. One port is assigned for interrupt level control and one other port is used for reading the rotary switches on the MCP. The rotary switches can be used as a general—purpose input channel for diagnostics, configuration selection, or automatic system boot with different configurations.

4—10.5VMEbus Interface

MCP VMEbus supports 8—, 16—, 32—bit, and unaligned data transfers. The extended, standard, and short I/O address modifier codes are implemented to interface to all existing VMEbus products. Each of the seven interrupt request signals can be connected to the implemented interrupt handler. A single—level bus arbiter and the bus arbitration, which has four bus release options, completes the VMEbus interface.

4—10.6MCP Function Switches And LEDS

The MCP contains four function switches and seven LEDs for board function control. The switches and LED functions are as follows:

a. A reset of all onboard I/O devices and the FPCP is enabled if the RESET switch is pushed to the “up” position. RESET is held active until the switch is in the “down” position. In addition, a local timer guarantees a minimum reset time of two to three seconds. Power fail and power up also force a reset (2—3 seconds) to start the board if the supply voltage is out of range (below 4.75 volts).

b. The ABORT switch, which provides an interrupt on a software—programmable level, is provided on the board to allow an abort of the current program, to trigger a self—test, or to start a maintenance program. ABORT is activated in the “up” position and deactivated in the “down” position.

c. The CACHE switch enables the 68030 onchip data cache with its 256 bytes when in the ”down” position. In the “up” position, the onchip cache is deactivated by hardware, overriding all software settings. MDP uses this switch in the “down” position.

d. The RUN/HALT (R/H) switch enables or disables local operation of the CPU and the FPCP. This switch can be used to debug multiprocessor software packages and to disable a CPU board in an application when a failure has occurred but power can’t be switched off. The processor is in the halt state if the switch is in the “up” position. Normal MDP operation is provided when the switch is in the “down” position.

e. The RUN LED is green if the processor is not in the halt state. It is red during the reset phase, and when the processor is in the halt state.

f. The SRAM LED is always lit yellow when the processor is accessing the local SRAM.

g. The EPROM LED is lit yellow when the processor accesses the EPROM area.

h. The bus request (BR) VME LED is lit yellow when the local processor requests bus mastership on the VMEbus.

i. The bus master (BM) LED is lit when the MCP is the current bus master.

j. The data strobe (DS) VME LED is lit whenever the processor has placed a data strobe on the VMEbus.

k. The DS VSB LED is lit whenever the processor has placed a data strobe on the VSB. Not applicable to MDP operations.

l. The rotary switches are 4—bit hexadecimal encoded. They are software control. Normal MDP operation is with the switches in the “F” position.

4−10.7 BERR Handling

The MCP contains a timeout counter to detect if an addressed device or memory does not respond with a DSACK to the CPU. The timeout is fixed, set to 70−80 microseconds, allowing slow VMEbus boards to communicate with the CPU.

4−11 Data Conditioning and Encoding PWA

Refer to figure 4−7 for the following DCEC functional description. The address select enables the control logic section of DCEC by matching address lines A23−A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines (A18−A01) are then used by the control logic to determine the function to be processed.

4−11.1 Data Format Conversion

DCEC performs data format and conversion on the command data channel. The command data is converted from NRZ−L to NRZ−L, −M, −S, or biphase−L data formats as commanded by MCP (via VMEbus interface). The NRZ output of the data format section goes to the encoder and a data select switch. The biphase output of the data format section goes to the data select switch. Biphase symbol asymmetry is less than 3% but is dependent upon the data clock being within +/−1.5% of a 50% duty cycle.

4−11.2 Convolutional Encoding

4−11.2.1 DCEC supports convolutional encoding for the SSHF (Shuttle) code (code 4). The Shuttle code is a rate 1/3 non−transparent. The generator functions for the Shuttle code are as follows:

Code 4: G1 = 1111001
G2 = 1011011
G3 = 1100101

4−11.2.2 The encoder is realized by multiplexing the output symbols such that the symbol corresponding to G1 precedes the symbol corresponding to G2 which precedes the symbol corresponding to G3.

4−11.3 Phased−Lock Loop

DCEC includes a phased−lock loop to support S−Band Shuttle modes. These modes require rate 1/3 encoding and biphase symbol formatting. Thus, a data clock rate of six times the data rate (6X) is required. Data clocks for these modes are limited to 32 kbps and 72 kbps. The phased−lock loop locks a 6X data clock to either of these data rates. The phased−lock loop uses a VCO running at 3.456 MHz, divides it down by 8 or 18 (8 for 72 kbps mode and 18 for 32 kbps mode). After dividing by 8 or 18, a 6X data clock is available for the biphase symbol format circuitry. The 6X data clock is then divided by 2 to provide the 3X clock required for rate 1/3 encoding. The 3X clock is then divided by 3 to provide the reference data clock for the phase detector of the phased−lock loop. The phased−lock loop bandwidth is 720 Hz and the acquisition time is less than 100 milliseconds.

4−11.4 Symbol Format Conversion

The output symbols of the encoder are Biphase−L converted. Biphase symbol formatting is accomplished by “EXclusive ORing” the encoder symbols with the inverted symbol clock. The biphase symbols are then reclocked with a 2X symbol clock (equal to the 6X data clock).

4−11.5 PN Spreading

4−11.5.1 DCEC generates all PN codes necessary to support forward PN code spreading techniques. DCEC has an external PN clock input (from TIME) to drive the PN code generator. The clock is normally 4 times the PN chipping rate and has a nominal frequency of 12 MHz. The clock also supports the Shuttle 11.232 Mcps chipping rate. The clock frequency is equal to the chipping rate for this mode (11.232 MHz) and is derived from an NCO and associated logic that resides on TIME.

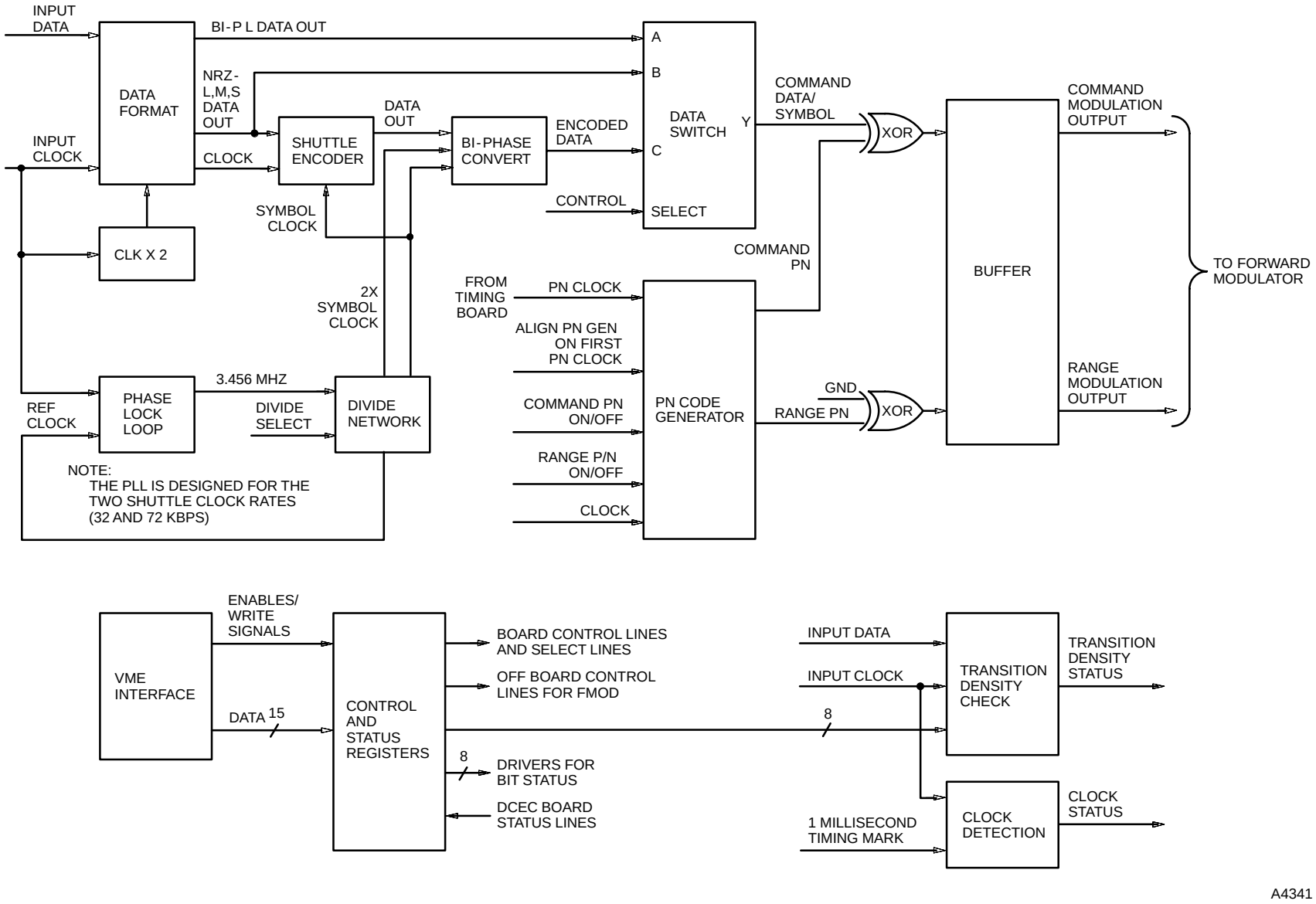

Figure 4—7. DCEC Functional Block Diagram

4—11.5.2 The PN epochs are initially aligned with the 1 - PPS signal. Synchronization is selected by an “Align PN” control bit in the DCEC control register. Toggling this control bit to and from its active state causes the PN code generator to be loaded in such a way that the first rising edge of a PN clock is the start of the epoch state and the next PN clock is the end of the epoch state. Thus, the accuracy of the 1 - PPS synchronization depends on the accuracy to which the first PN clock can be aligned with the 1 - PPS. PN chip asymmetry is less than or equal to 0.01 of a PN chip.

4—11.6 Clock Detection

DCEC has a clock detection circuit that checks whether the input clock has positive transitions at a rate greater than 97 per second. Clock rates less than 97 Hz are considered to be in error. The output of this circuit is represented by the “Clock Error” status bit and is latched on any error and cleared after being read by the MCP. Data is clamped to a logical “1” when a clock error is detected, but this can be overridden by the “Clamping Override” bit in the control register.

4—11.7 Data Presence Detection

This circuit detects data transitions. The circuit shows an error in the DCEC VMEbus status register if no transition has been detected since the last time this register was read.

4—11.8 DCEC Registers

The control register is a read/write register used to control data formats, select encoders, and select/control other board functions. The control register address offset is 1000A (hex). This register is also used to output the high/low rate and range channel disable control signals to FMOD. The forward modulator status register is a read - only register that provides status of forward modulator. The forward modulator status register address offset is 10008 (hex). The LED register provides BIT status and has read/write capabilities. The register uses inverted logic in that a “1” represents a turned - off light and a “0” represents a turned - on light. The address offset of the LED register is 10004 (hex).

4—12 Timing Generator PWA

Refer to figure 4 - 8 for the following TIME functional description. The address select enables the control logic section of TIME by matching address lines A23 - A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines (A18 - A01) are then used by the control logic to determine the transfer function to be processed.

4—12.1 IRIG Decoding

TIME provides the capability of decoding unmodulated IRIG - B data into components of seconds, minutes, hours, and days, and to buffer these signals to the data lines on the VMEbus when enabled by the control logic. The IRIG - B data is updated and written to RAM between the 0 msec and 500 msec marks. The data is valid for reading from RAM between the 500 msec and 0 msec marks. The time components are in binary - coded decimal (BCD) format.

4—12.2 1553 Interface

TIME provides a transformer - coupled 1553 interface between the VMEbus and the P2 connector. The interface to the P2 connector consist of two transmit/receive transformers and the remote terminal address inputs. The interface to the P1 connector consists of the address and data lines to read/write to 1553 control/status registers and RAM.

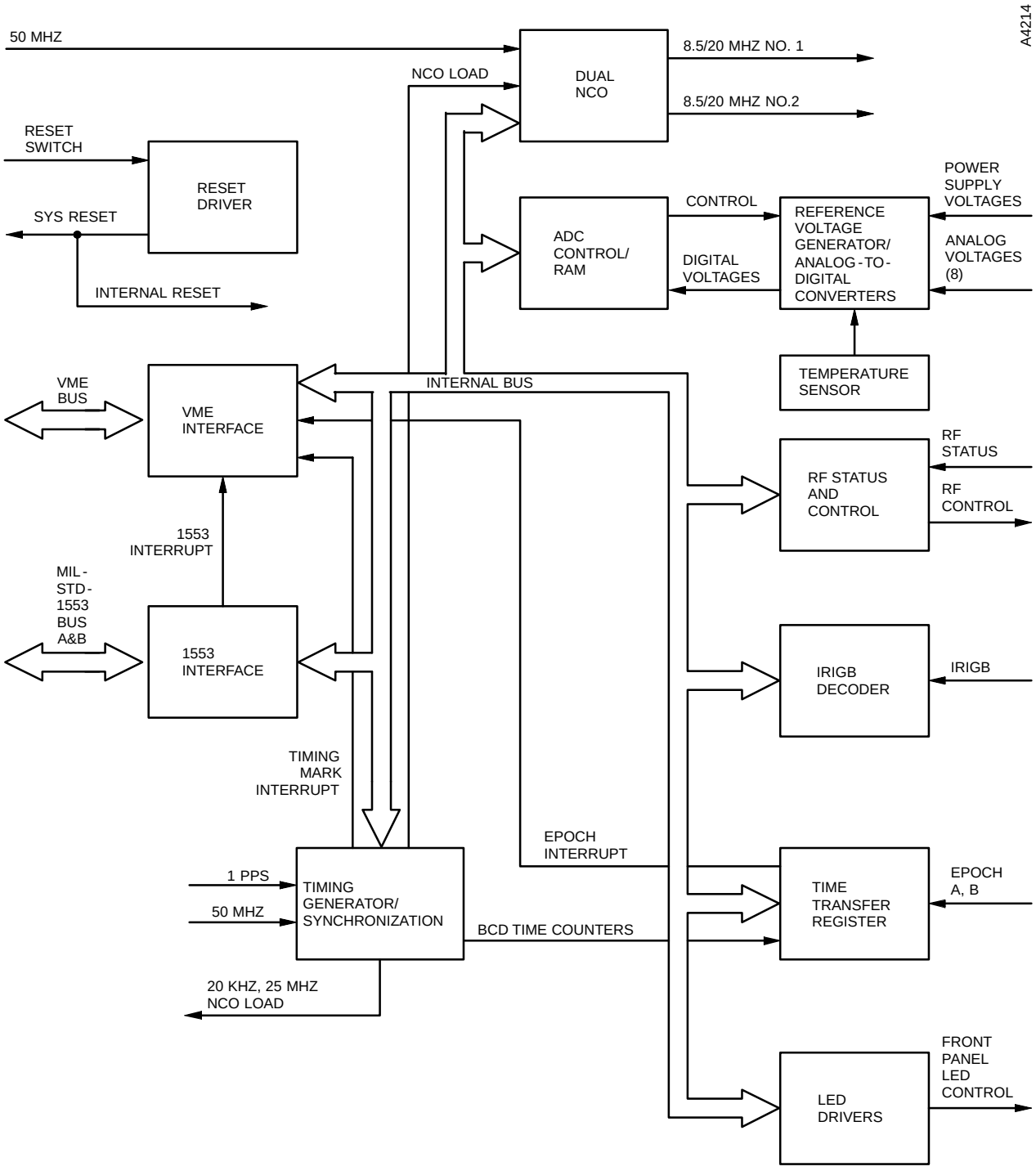

Figure 4—8. TIME Functional Block Diagram

4−12.3Time Mark Generation

TIME generates 1, 10, 100, 1000, and 20,000 PPS time marks based on the 50−MHz input in sync with the 1−PPS external signal. The time marks have a duty cycle of 20% and are valid on the falling edge of the pulse. A status indicating the detection of a time synchronization error between the 1−PPS external and the 1−PPS generated is provided in the TIME status word. The time synchronization error is set if the 1−PPS external and 1−PPS internal signals differ by more than one 50−MHz clock cycle. A time resynchronization may be commanded through the TIME control register. There is also a flag that is set when the resynchronization process is complete.

4−12.4Interrupt Generation

TIME provides interrupt to the VMEbus consisting of the generated time marks, the 1553 interrupt, and the selected epoch interrupt. Any or all of the interrupts can be masked through the interrupt mask register. The interrupts are divided into two separate groups: time interrupts and other interrupts. Each group has a programmable vector in which the upper nibble is determined by the interrupt vector register. The lower nibble is determined by the interrupt generated. The time interrupts interrupt the microprocessor with a level 6 interrupt and the other interrupts with a level 3 interrupt.

4−12.5Epoch Count Generation

TIME provides the time difference between the command channel epoch or range channel epoch and the 1−PPS signal with 100 nanosecond resolution when enabled by control logic. This time difference is valid upon the epoch interrupt of the microprocessor. The difference components are in BCD format. The epoch is selectable between command and range through the TIME control word.

4−12.6NCO Outputs

TIME provides two NCOs that are to be controlled from the VMEbus. The NCO's have a sampling frequency of 50 MHz and a 22−MHz lowpass filtered analog output of these NCOs is available through coaxial connectors J1 and J2.

4−12.7Analog−To−Digital Generation

4−12.7.1 TIME provides a digital measurement of various analog voltages to the data lines on the VMEbus when enabled by control logic. There are 16 possible measurements, and the measurements are updated and written to RAM between the 800 msec and 0 msec marks; therefore, the measurements are valid for reading from RAM between the 0−msec to 800−msec marks. Channels 0−7 are predefined and channels 8−15 are user defined. The analog level value register output value is dependent upon the channel being read. The output range is +/− 10 volts, and the LSB is equal to 4.88 millivolts. The output is in offset binary format meaning 0000H = −10 volts, 0800H = 0 volts, and 0FFF = +10 volts.

4−12.7.2 The channels are defined as follows: channel 0 is the −5.2 Vdc and +5 Vdc supply sum, channel 1 is the −12 Vdc and +12 Vdc supply sum, channel 2 is the −15 Vdc and +15 Vdc supply sum, channel 3 is ground, channel 4 is the −6.2 Vdc reference, channel 5 is the +6.2 Vdc reference, channel 6 is the temperature sensor, and channel 7 is the RF 5 Vdc supply. The temperature sensor voltage to degrees C conversion is as follows: 15.0°C = +5.764 volts, 20.0°C = +5.864 volts, 25.0°C = +5.964 volts, 30.0°C = +6.064 volts, etc.

4−12.8 Miscellaneous Registers and Control

TIME test point register provides up to eight test points on the TIME via the P2 connector controllable from the VMEbus. Each point is cleared or set through the corresponding bit in the test point register. The TIME driver register provides eight bits of control adjustable by control from the VMEbus. This register interfaces to the P2 connector to drive various signals. The TIME also

provides the capability of reading a reset switch from the P2 connector and drive SYSRESET* on the P1 connector to reset the system when this switch is closed for a minimum of 200 msec.

4−12.9 RF Status and Control

The RF modules provide TTL level RF status signals which provide up to 8 bits of RF status information to the VMEbus upon command. Subsequentyly, 8 bits of adjustable control are generated for use by the RF modules.

4−13 Synthesizer PWA

Refer to figure 4−9 for the following SYNTH functional description. SYNTH accepts a 10−MHz reference signal from an external interface and splits it with one portion output to a test point on the maintenance panel and the other for internal processing. The 10−MHz signal is sent through a BPF with a center frequency of 10 MHz and a bandwidth of 1 MHz. The filtered signal is buffered and split with one portion for status monitoring and the other for further processing in a 140−MHz PLL. The 140−MHz PLL is performed by taking the output of a 140−MHz VCXO and dividing it by 14. The resultant 10−MHz signal is phase detected with the 10−MHz reference input. The phase error signal is put through a loop filter which drives the 140−MHz VCXO. SYNTH produces the following clocks and timing signals:

a. A 70−MHz LO signal is produced by dividing the 140−MHz phased−locked signal by 2.

b. A 300−MHz LO is produce by upconverting the 20−MHz NCO input using a 280−MHz signal. The 280−MHz signal is produced by multiplying the 140−MHz signal by 2.

c. A 50−MHz clock is produced by adding the 20−MHz NCO input and the 10−MHz output of the divide−by−14 network in the 140−MHz PLL. The resultant 30−MHz signal has a 50−MHz harmonic present, which is 10 dB below the 30−MHz signal. A 50−MHz filter is used to reject the undesirable signals leaving the 50−MHz component.

d. A 61.5−MHz LO and 61.5−MHz clock are produced by high side downconverting the 61.5−MHz VCXO to 8.5−MHz using a 70−MHz produced signal. The 70−MHz signal is produced by dividing the 140−MHz PLL signal by 2. The 8.5−MHz signal passes through a bandpass filter (8−MHz bandwidth) and then is divided by 17 to produce 0.5 MHz. The 0.5−MHz downconversion signal is phase compared to another 0.5−MHz signal produced by dividing the 10−MHz signal (from the 140−MHz PLL) by 20. The resulting phase error output is then put through a loop filter which drives the 61.5−MHz VCXO.

e. SYNTH produces an 8.5−MHz output signal which is a direct tapoff of the 8.5−MHz signal produced in the 61.5−MHz PLL.

f. The variable 61.5−MHz LO output is produced by subtracting 8.5−MHz NCO input from the internally generated 70−MHz signal. The 70−MHz signal is produced by dividing the 140−MHz PLL signal by 2.

g. SYNTH provides status two ways: (1) an LED mounted on the PWA which turns on to indicate the 61.5−MHz PLL, 140−MHz PLL, and 10−MHz reference input are correct, and (2) three output status lines indicating the same.

4−14 Forward Modulator

Refer to figure 4−10 for the following FMOD functional description. FMOD operates in two general modes: low data rate mode (rates less than or equal to 6 Mbps) and high data rate mode (rates greater than 6 Mbps).

4−14.1 70−MHz UQPSK Modulator

In the low−rate mode, both the command and range data are fed to the modulator which UQPSK modulates the 70−MHz LO. The range channel normally operates at −10 dB relative to the command channel signal power. Alternatively, the range channel can be disabled (turned off) so it is not modulated onto the IF carrier. A 70−MHz bandpass filter is used at the modulator output to

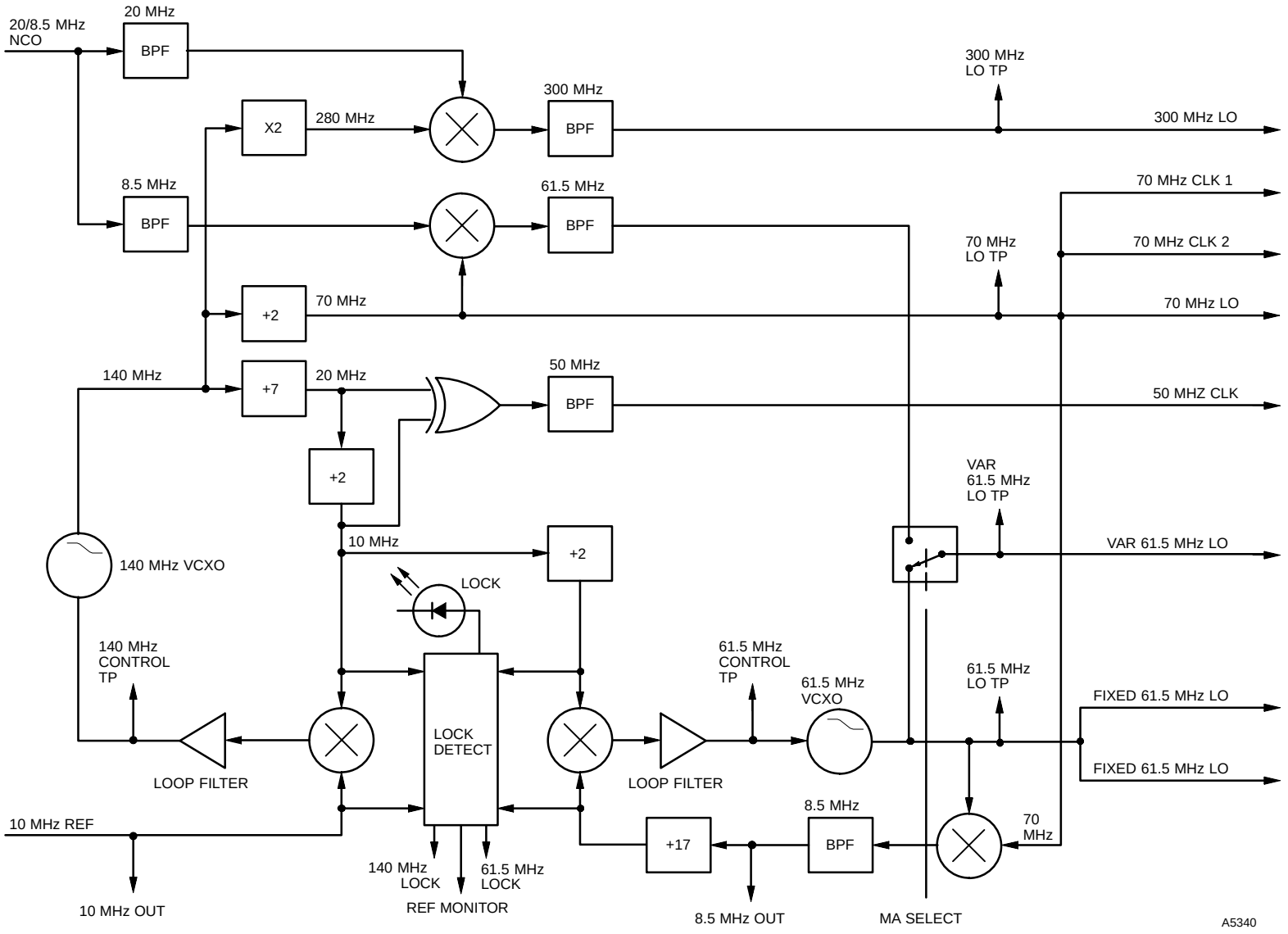

Figure 4—9. SYNTH Functional Block Diagram

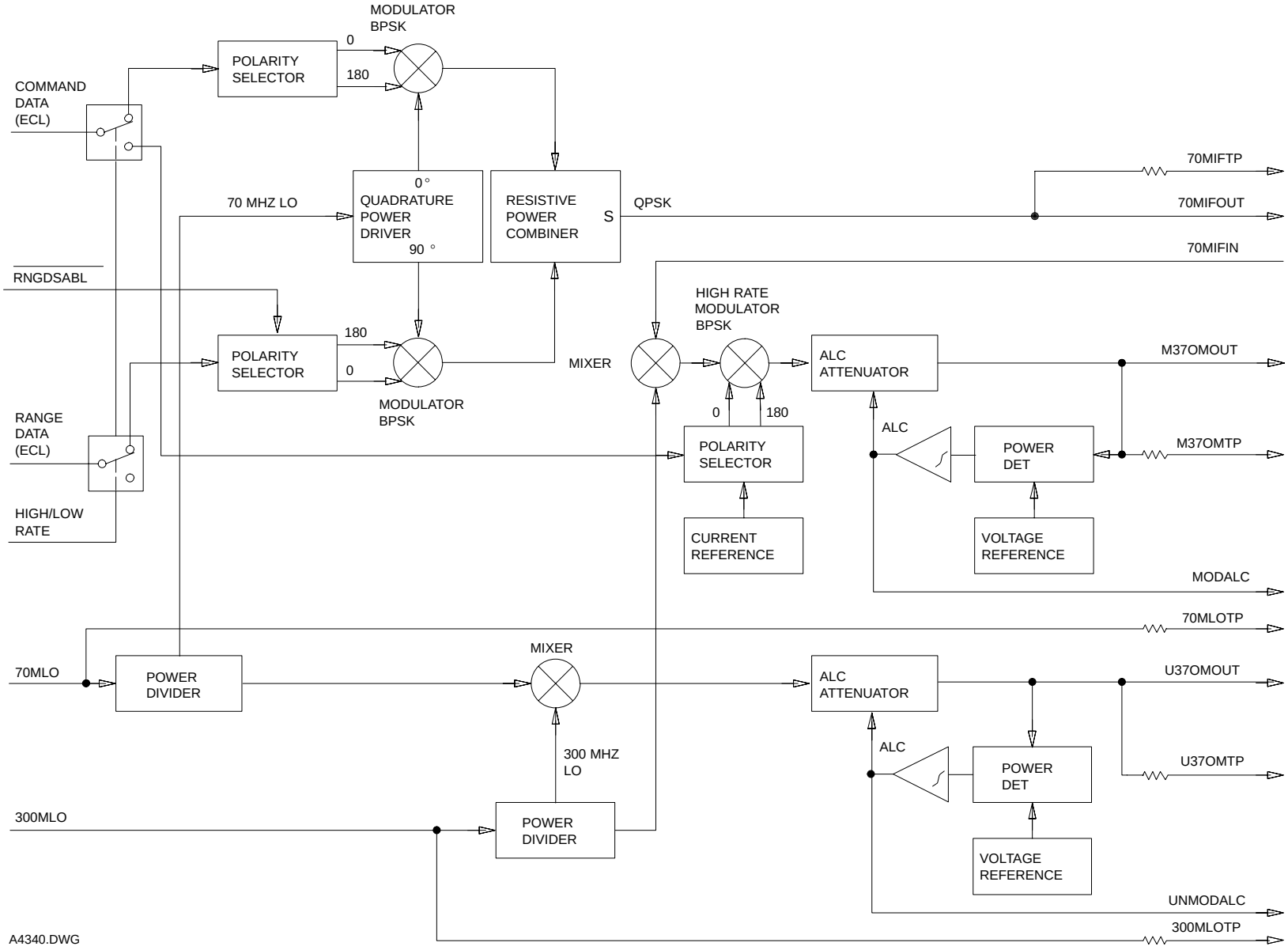

Figure 4—10. FMOD Functional Block Diagram

establish the maximum bandwidth for a range of modulation conditions (i.e., to restrict the transmitted spectrum). This bandpass filter has a fixed bandwidth of 12 MHz and a center frequency of 70 MHz. The 70 MHz IF ouput of the UQPSK modulator is routed off−board to the GMOD PWA.

4−14.2 Modulated 370−MHz IF Output (Low Data Rate Mode)

A 70 MHz IF input is accepted from the GMOD PWA. For PSK modes, this is the 70 MHz IF ouput of the FMOD UQPSK modulator; for PM modes, it is the output of the GMOD phase modulator. This signal is upconverted to 370 MHz, using the 300−MHz LO input from SYNTH. The upconverter output is then filtered again to produce the 370−MHz IF output. The 300−MHz LO is variable to allow Doppler precompensation of the modulated 370−MHz IF output. In this mode, the high rate BPSK modulator is not used. The 370−MHz bandpass filter used in the translator stage of FMOD has a center frequency of 370 MHz and a 30−MHz bandwidth at the 3−dB level.

4−14.3 Modulated 370−MHz IF Output (High Data Rate Mode)

In the high−rate mode, the 70−MHz UQPSK modulator is turned off and passes the 70−MHz carrier on to be upconverted to a 370−MHz carrier. The upconverter uses the 300−MHz LO input from SYNTH. The 300−MHz LO is variable to allow Doppler precompensation of the modulated 370−MHz IF output. The command data is fed to the high−rate BPSK modulator, which directly modulates the 370−MHz carrier. The high−rate BPSK−modulated 370−MHz IF output is unfiltered.

4−14.4 Unmodulated 370−MHz IF Output

The unmodulated 370 MHz IF output is obtained by mixing the 300 MHz LO with the 70 MHz LO. The unmodulated 370 MHz IF output is filtered following the frequency conversion stage. The 300 MHz LO is variable to allow Doppler precompensation of the unmodulated 370 MHz IF output.

4−14.5 Automatic Level Control

Separate ALC circuits are provided for the modulated and unmodulated 370−MHz IF outputs. The ALC circuits provide an optimum 0 dBm IF output level.

4−15 GN Modulator PWA

Refer to the GN Modulator Operations and Maintenance Manual for information about the GMOD PWA.

4−16 Modulator/Doppler Predictor External Interface Description

Refer to table 4−3 for a description and connector pin identification of the external interfaces for the Modulator/Doppler Predictor.

4−17 Modulator/Doppler Predictor Internal Interface Description

During Level 1 maintenance, the only accessible internal interface signals are located on the maintenance panel and described in section 3, table 3−2. Descriptions of the remaining internal interface signals are not applicable to Level 1 maintenance; therefore, this paragraph is not applicable.

4−18 Mechanical Components

This paragraph is not applicable to the Modulator/Doppler Predictor.

Table 4—3. External Interface Signal			
CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J101	A B C	115VAC CHASSIS GND 115VAC RTN	Site—supplied source power.
J102	1 2	370 MHZ IF MODULATED SHIELD	370—MHz modulated IF signal output used for all forward service configurations.
J103	1 2	N/A SHIELD	Not used.
J104	1 2	10 MHZ SHIELD	Common Time and Frequency System (CTFS) reference input signal used to synchronize the MDP's 140—MHz SYNTH VCXO.
J105	1 2	1PPS CTFS SHIELD	CTFS 1 Hz reference time mark used to synchronize the MDP's 50—MHz TIME clock.
J106	1 2	TOY CTFS SHIELD	CTFS unmodulated IRIG—B (time of year) data signal.
J107	A B C	1553 BUS 1553 BUS RTN SHIELD	MIL—STD—1553B digital time division command/response multiplex data bus (A1).
J108	A B C	1553 BUS 1553 BUS RTN SHIELD	MIL—STD—1553B digital time division command/response multiplex data bus (A2).
J109	01 02 03	CMDCLK+ CMDCLK— SHIELD	Complimentary balanced differential TTL or MC10125 differential receivers or equivalent ECL command clock input at the selected bit stream rate.
J109	04 05 06	CMDDATA+ CMDDATA— SHIELD	Complimentary balanced differential TTL or MC10125 differential receivers or equivalent ECL command data bit stream input.
J109	31 32 33 34 35 36 37	RTA0 RTA1 RTA2 RTA3 RTA4 RTAP (parity) RTAR (return)	1553 Bus MDP remote terminal address (RTA) select input.

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Section 5 — Maintenance

5−1 Introduction

5−1.1 This section contains information to aid personnel in the Level 1 maintenance of the Modulator/Doppler Predictor. Level 1 maintenance is defined as those tasks permitting a technician (with the unit installed in the equipment rack) to fault isolate a failure to the chassis line replaceable unit (LRU), remove and replace the faulty LRU, and restore the unit to operation within a specified time. Major component LRUs are listed in table 5−1. Before performing any procedures, refer to paragraph 3−5 for warnings aimed at preventing death or injury and equipment damage.

5−1.2 Level 2 maintenance instructions are not provided for in this manual. Repairable LRUs are sent to the depot for repair. Level 2 maintenance is defined as those tasks permitting a technician (with the unit removed from the equipment rack and taken to the HMD area) to fault isolate the failure to the LRU. Depot level maintenance consists of repairing failed LRUs to the piece part, repairing any other discrepancy not discovered at the Level 1/2 maintenance level, equipment refurbishment and performing major modifications to the equipment, when required. The MDP manufacturer maintains depot maintenance facilities for all LRUs. Refer to table 5−2 for the MDP maintenance concept.

Table 5−1. Replaceable LRUs

NOMENCLATURE	PART	LRU	LEVEL
Modulator/Doppler Predictor	7472300		
Timing Generator PWA	7473000−502	X	1, 2
Modem Control Processor PWA	7473600	X	1, 2
Synthesizer PWA	7474600−500	X	1, 2
Data Conditioning and Encoding PWA	7473800−501	X	1, 2
Forward Modulator PWA	7474800	X	1, 2
GN Modulator PWA	1547558	X	1, 2
Power Supply No. 1	LFQ−27−1	X	1, 2
Power Supply No. 2	RMV223B−2330−0450	X	1, 2
Tubeaxial Fan	A47−B15A−15T3−000	X	1, 2
Lamp Cartridge (green, DS1 only)	CF296CWPG6−120VAC−B	X	1, 2
Lamp Cartridge (green)	507−4857−3732−500	X	1, 2
Lamp Cartridge (red)	507−4757−3731−500	X	1, 2
Lamp Cartridge (amber)	507−4957−3733−500	X	1, 2
Lampholder	DH0−30Y−D86BWC	X	2
Pushbutton Switch	W403PGR	X	2
Toggle Switch (AC POWER)	MS24659−22F	X	2
Toggle Switch (LOCAL/REMOTE)	MS24658−23F	X	2
Circuit Breaker	MS25244−10	X	2
Harness Assembly	7472360		2

Table 5—2. Modulator/Doppler Predictor Maintenance Concept		
LEVEL 1 MAINTENANCE	LEVEL 2 MAINTENANCE	DEPOT LEVEL
TASK	TASK	TASK
* Detect malfunctions * Isolate LRU * Remove/replace LRU * Preventive maintenance	* Localize fault to subassembly * Isolate LRU * Remove/replace LRU * Preventive maintenance	* Repair LRU
Timing Generator Modem Control Processor Synthesizer Data Conditioning and Encoding Forward Modulator GN Modulator Power Supply No. 1 Power Supply No. 2 Lamp Cartridges (all) — Discard Tubeaxial Fan — Discard		Repair Repair Repair Repair Repair Repair Repair Repair
	Harness Assembly Lampholders (all) — Discard Front Panel Switches — Discard Circuit Breaker — Discard	

5—2 Performance Standards

Minimum performance standards for Level 1 operation and maintenance are detailed in paragraph 5—6: operational verification procedure. If the MDP fails to meet any of the operational performance steps, perform MDP fault isolation procedures (paragraph 5—4).

5—3 Test And Adjustment Procedures

Test and adjustment procedures for the MDP include only power supply adjustments. The following procedure describes how to adjust PS1 and PS2.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

d. Applying pressure to bottom cover towards unit chassis, use a flat—tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

e. Carefully lower bottom panel to gain access to power supplies.

f. Refer to the following list of voltage adjustments and to figures 5 - 1 and 5 - 2 for location of adjustment potentiometers when performing power supply voltage adjustments.

Power Supply	Adjustment	Test Point	Voltage
PS1	V - ADJ #1	+5	+5.0 +/ - .25 Vdc
PS1	V - ADJ #2	+15	+15.0 +/ - .5 Vdc
PS1	V - ADJ #3	- 15	- 15.0 +/ - .5 Vdc
PS1	V - ADJ #4	+5RF	+5.0 +/ - .25 Vdc
PS2	V1	- 5.2	- 5.2 +/ - .25 Vdc
PS2	V2	+12	+12.0 +/ - .25 Vdc
PS2	V3	- 12	- 12.0 +/ - .25 Vdc

WARNING

When adjusting voltages, beware of power terminals. Voltage present may cause DEATH or injury.

g. Set AC POWER ON/OFF switch to ON.

h. Connect digital voltmeter to respective power supply voltage test points on the maintenance panel and adjust voltage to within specifications. If specifications cannot be achieved, replace faulty power supply and repeat this procedure.

i. Set AC POWER ON/OFF switch to OFF.

j. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

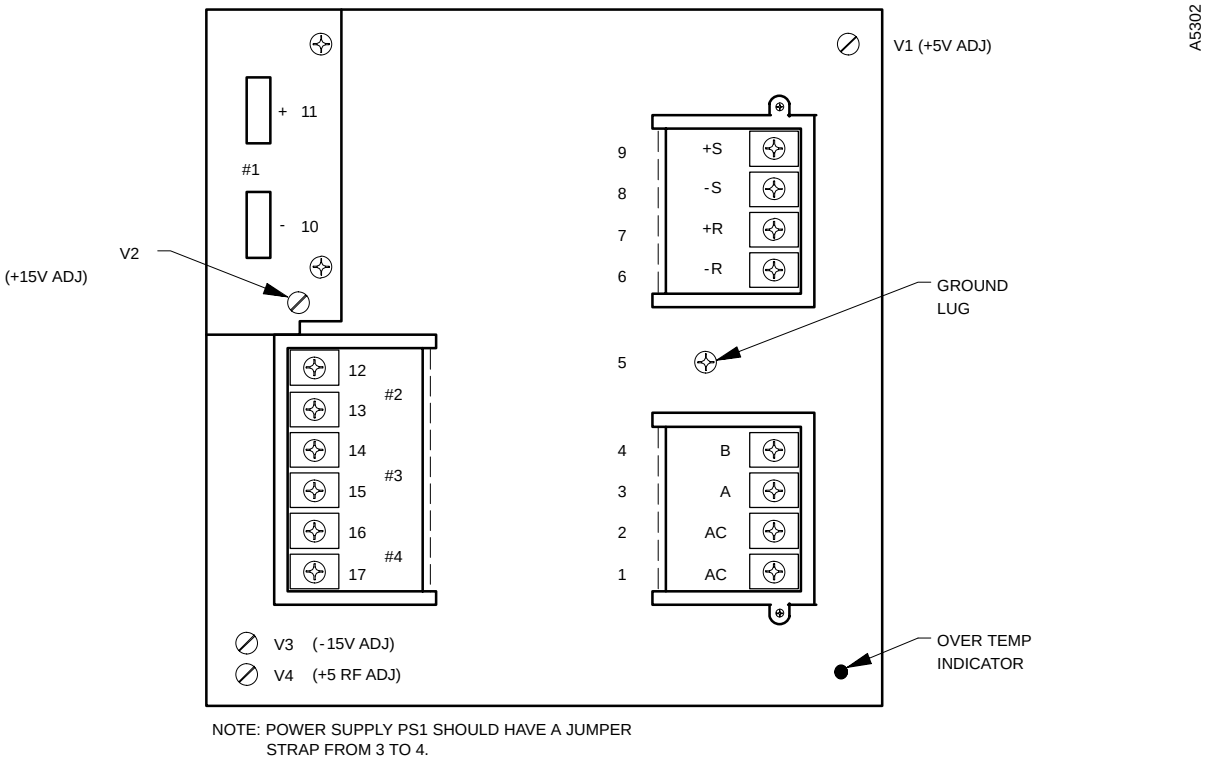

Figure 5 - 1. Power Supply No. 1 Voltage Adjustments

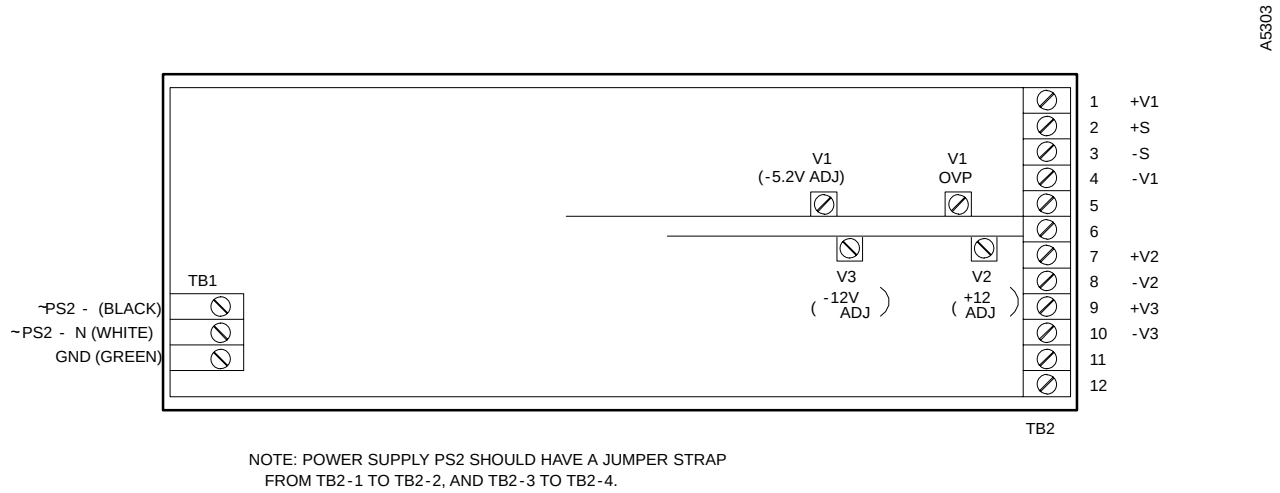

Figure 5 - 2. Power Supply No. 2 Voltage Adjustments

k. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

l. Tighten four front - panel captive screws to the cabinet assembly.

m. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

5—4 Fault Isolation (Troubleshooting)

Information to aid fault isolation within MDP to an LRU is presented in table 5 - 3. This procedure is performed at the unit level with MDP LOCAL/ REMOTE switch set to the LOCAL position. Before performing any procedures, refer to paragraph 3 - 5 for safety information. Procedures for troubleshooting the MDP may be used in conjunction with troubleshooting procedures in the respective O&M manuals (see section 3, paragraph 3 - 8). If an LRU in the MDP is faulty, refer to paragraph 5 - 7 for removal/replacement (R/R) procedures. The line maintenance technician (LMT) replaces the faulty LRU with a spare and sends the faulty assembly to the HMD for fault verification prior to shipment to the manufacturer for depot repair.

WARNING

Before attempting to perform any troubleshooting procedures, ensure that power has been removed (when possible) to prevent injury or DEATH from electric shock. It is recommended that at least two people are present at all times when working on energized equipment.

Table 5—3. Fault Isolation			
STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
1.	Ensure ON/OFF switch is in the OFF position and the LOCAL/ REMOTE switch is in the LOCAL position.	All front—panel indicators are turned off.	Faulty power switch
2.	Loosen the front panel screws, slide the MDP forward until rail—guide locks are set to locked position.		
3.	Loosen top—cover screws and raise top cover to gain access to PWAs.	All PWA indicators are turned off.	
4.	Place the ON/OFF switch to the ON position.	The AC POWER indicator turns on. The cooling fan blowers turn on. The DC POWER indicators turn on.	Site—power not available CB101 faulty POWER ON indicator/ lampholder faulty Faulty fan Faulty indicator/lampholder Faulty power supply
5.	Using a digital multimeter, monitor dc power supply voltages at the maintenance panel.	See section 1, table 1—3.	Faulty power supply (Adjust if possible; see paragraph 5—3)
6.	Using an oscilloscope, monitor the 1PPS EXT test point at the maintenance panel.	See section 1, table 1—3.	Site—supplied 1PPS signal not available
7.	Using a frequency counter, monitor the 10 MHZ test point at the maintenance panel.	See section 1, table 1—3.	Site—supplied 10—MHz signal not available SYNTH PWA faulty

Table 5—3. Fault Isolation (Continued)

STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
8.	Press the RESET switch on maintenance panel.	The TEST indicator turns on and the NORMAL indicator turns off (except for 1—second test) for duration of the confidence BIT; the FAULT indicator remains turned off (except for 1—second test). At completion of the confidence BIT, the NORMAL indicator turns on and the TEST indicator turns off.	Faulty indicator/lampholder View the DCEC PWA LEDs and replace faulty PWA/ LRU identified by the DCEC PWA indicators (the FMOD PWA LED may indicate a failure of the GMOD PWA) View the MCP PWA and replace the MCP PWA if the RUN LED is turned on RED. If after replacing the MCP PWA, this fault continues to occur, systematically replace each PWA on the VMEbus until the PWA with the VME fault is found. A fault indication (FAULT indicator turned on and MCP PWA RUN indicator turned on red) may be induced by a failure in the ADPE interfaced to the 1553 bus
9.	Press the BIT INITIATE switch.	The TEST indicator turns on and the NORMAL indicator turns off for duration of the extended BIT; the FAULT indicator remains turned off. At completion of the extended BIT, the NORMAL indicator turns on and the TEST indicator turns off.	View the DCEC PWA LEDs and replace faulty PWA/LRU identified by the DCEC PWA indicators (the FMOD PWA LED may indicate a failure of the GMOD PWA) View the MCP PWA and replace the MCP PWA if the RUN LED is turned on RED
10.	Perform Level 1 equipment group maintenance pro— cedures to further isolate chassis fault.	Refer to applicable Level 1 O&M manual (see section 3, paragraph 3—8).	
11.	Replace chassis with good MDP resident in STGT Electronics System Test Set (in the HMD area) if faulty LRU cannot be identified within Level 1 specified repair time.		

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5–5 Preliminary Fault Isolation Steps

As a first step in fault isolation, perform the following preliminary steps. If any preliminary step leads to a possible fault, after correcting that possible fault, conduct paragraph 5–6 and verify that the fault(s) still exist.

a. Ensure all mechanical connections are secure. Check for improperly mated connectors, improperly seated PWAs, and evidence of physical damage.

b. Ensure power is available to unit.

c. Ensure (as nearly as possible) that all other equipment in, or associated with, the MDP is operating properly.

d. Observe the front–panel indicators and PWA LEDs for proper operation.

5–6 Operational Verification

This paragraph contains procedures that checkout and confirm the MDP's Level 1 operational status while in local control. Before proceeding with any procedures involving the MDP, refer to paragraph 3–5. Unless otherwise specified, all actions will take place from the MDP front panel. Upon any step which does not give a normal indication, stop operational verification procedure and proceed to table 5–3 and perform the fault isolation procedures.

a. Ensure paragraph 5–5, Preliminary Fault Isolation Steps has been completed in its entirety.

b. Place the ON/OFF switch to the OFF position.

c. Place the LOCAL/REMOTE switch to the LOCAL position.

d. Loosen the four captive screws holding the MDP in the cabinet.

e. Slide the unit forward until the rail–guide locks are set to the locked position.

f. Using a flat–tipped screwdriver, loosen four captive screws securing top cover to maintenance panel. Raise top cover to gain access to PWAs.

g. Place the ON/OFF switch to the ON position and verify the following:

   (1) AC POWER indicator turns on.

   (2) Cooling fan blowers turn on.

   (3) All seven DC POWER indicators turn–on.

   (4) TEST indicator turns on.

   (5) All front–panel indicators turn on for a 1–second period.

   (6) All STATUS indicators are turned off (after item 5 above).

h. Verify the TEST indicator turned off after approximately 10 seconds, the FAULT indicator remains turned off, and the NORMAL indicator turns on.

i. Verify the MCP PWA RUN LED is turned on green.

j. Verify all DCEC PWA LEDs are turned off except the PHASE LOCK LED which may or may not be turned on.

k. Verify the SYNTH PWA LOCK LED is turned on.

l. Press the BIT INITIATE switch and verify the TEST indicator turns on.

m. Verify the TEST indicator turns off after approximately 10 seconds, the FAULT indicator remains turned off, and the NORMAL indicator turns on.

n. Verify the MCP PWA RUN LED is turned on green.

o. Verify all DCEC PWA LEDs are turned off except the PHASE LOCK LED which may (only ON when processing 32 Kbps data) or may not be turned on.

p. At the maintenance panel, press the RESET switch.

q. Verify all STATUS indicators are turned off (except as per step r) except the TEST indicator which is turned on while the confidence BIT executes.

r. Verify all front—panel indicators turn on for a 1—second period.

s. Verify the TEST indicator turns off after approximately 10 seconds, the FAULT indicator remains turned off, and the NORMAL indicator turns on.

t. Verify the MCP PWA RUN LED is turned on green.

u. Verify all DCEC PWA LEDs are turned off except the PHASE LOCK LED which may or may not be turn on.

v. Verify the SYNTH PWA LOCK LED is turned on.

w. Close top cover and using a flat—tipped screwdriver, tighten four top cover captive screws to maintenance panel.

x. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

y. Tighten four front—panel captive screws to the cabinet assembly.

z. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

aa. Further MDP operational verification is performed by utilizing the MTG. Refer to O&M manual applicable to suspect MDP equipment group (see section 3, paragraph 3—8); otherwise, proceed with step ab.

ab. Place the REMOTE/LOCAL switch to the REMOTE position. Notify the TOCC2 operator that the MDP is online and ADPE operation (remote mode) is enabled.

5—7 Removal/Replacement

The following procedures provide removal and replacement instructions for MDP major components. The procedures are presented in a step—by—step format to facilitate user comprehension and simplify task complexity. Tools or equipment required for removal and replacement of MDP components are identified in the text, where applicable. These procedures assume that MDP has been health tested in accordance with the procedures in paragraph 5—4 and that one or more LRUs have been identified as defective.

WARNING

Before attempting to perform any removal/replacement procedures, ensure that power has been removed (when possible) to prevent injury or DEATH from electric shock. It is recommended that at least two people are present at all times when working on energized equipment.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5–8 PWA Replacement

The MDP PWAs are mounted in a card cage accessible from the top of the unit. The primary ac power must be turned off before replacing a PWA. When inserting PWAs, care must be used to ensure that connectors are properly aligned before applying engaging force. Perform the following procedure when a defective PWA is identified.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Using a flat–tipped screwdriver, loosen four captive screws securing top cover to maintenance panel. Raise top cover to gain access to PWAs.

e. When applicable, tag all RF cable(s) connected to top of PWA to be replaced.

f. Disconnect tagged RF cables from suspect PWA by gently pulling snap–on connector from PWA RF receptacle.

g. Using a flat–tipped screwdriver, loosen two captive screws securing PWA to chassis.

h. Grasping both PWA handles and pushing outward, unseat and remove PWA.

NOTE

For the MCP PWA, SP7472300–XXX IC chips (J21, J23, J25, and J27) must be removed from faulty PWA and inserted onto the new MCP PWA. Perform the IC chip removal and insertion paragraph 5–9 prior to installing the new MCP PWA.

Figure 5–3 shows the MCP PWA jumper locations. Refer to table 5–4 for jumper descriptions and settings. Also shown are the four EPROM socket locations for SP7472300–XXX IC chip set and proper installation alignment.

i. Install replacement PWA in its appropriate slot and apply pressure to ensure proper seating.

j. Using a flat–tipped screwdriver, secure PWA to chassis with captive screws.

k. When applicable, reconnect tagged RF cables to replacement PWA by gently seating RF cable to PWA SMB connector.

l. Inspect unit to ensure proper reassembly.

m. Close top cover and using a flat–tipped screwdriver, tighten four top cover captive screws to maintenance panel.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front–panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5–6 Operational Verification to verify MDP operability.

5–9 IC Chip Replacement

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting pats or assemblies.

a. Place faulty MCP PWA on an ESD approved work bench.

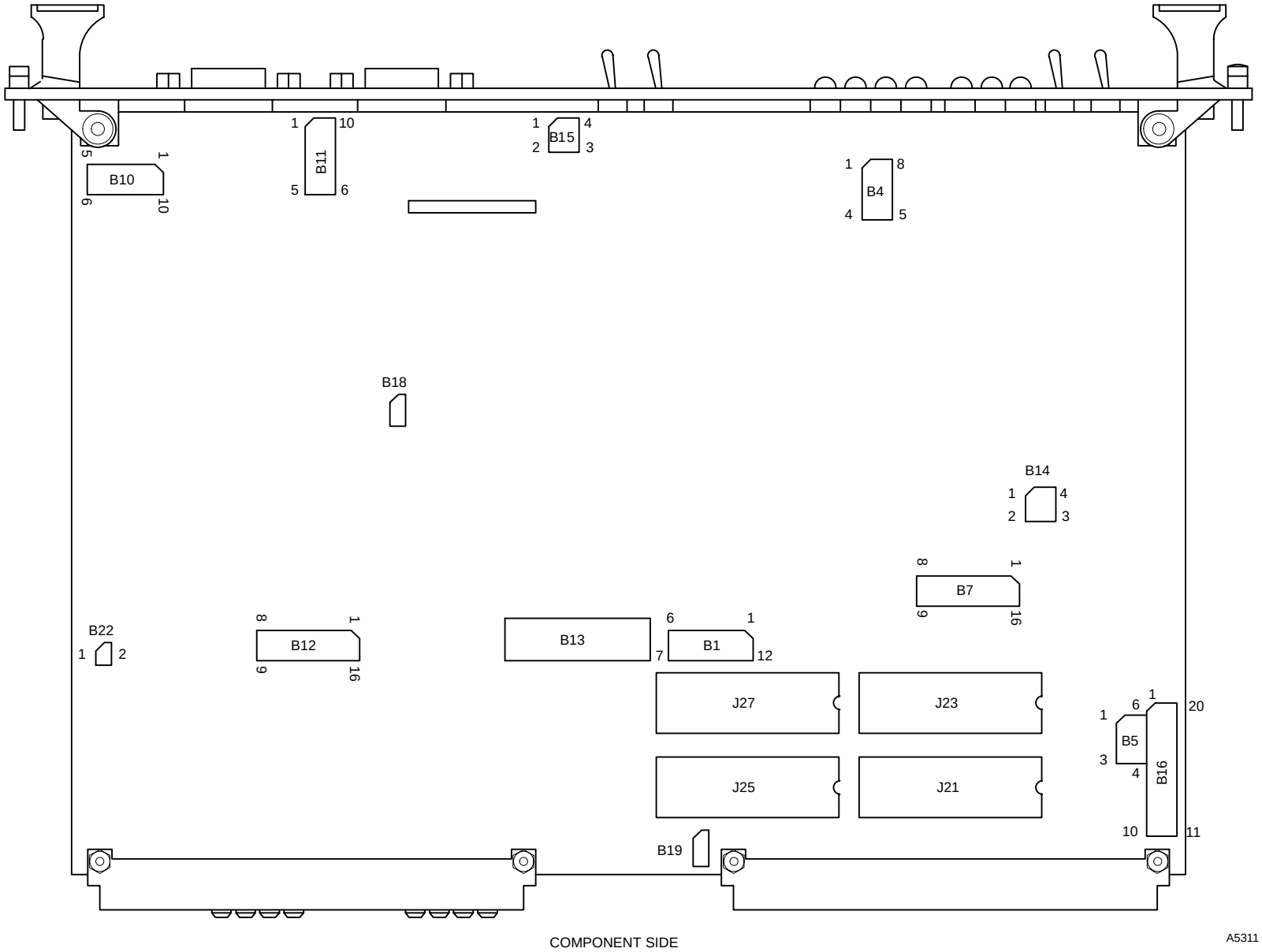

Figure 5 - 3. MCP PWA Component Location Diagram

Table 5—4. MCP Jumper Configurations

JUMPER BLOCK	JUMPER BLOCK DESCRIPTION	JUMPERS INSTALLED	CONFIGURED JUMPER FUNCTION
B1	Address comparator for SRAM	1 – 12 3 – 10 5 – 6 8 – 9	1 Mbyte local SRAM
B4	Access time selection for EPROM area	 3 – 6 4 – 5	200 ns EPROMS
B5	Clock to bus Reset to bus Reset from bus	1 – 6 2 – 5 3 – 4	Clock enabled to bus Reset enabled to bus Reset enabled from bus
B7	EPROM area address decoding	1 – 16 2 – 15 3 – 14 4 – 13	EPROM type: 27C010 Organization: 128K x 8
B10	Serial interface MPCC1 RS232 control	2 – 3 4 – 7 5 – 6	DSR – DSR (OUT) DCD – CTS (IN) DTR – DTR (OUT)
B11	Serial interface MPCC2 RS232 control RS422/485 control	2 – 3 4 – 7 5 – 6	– DSR – CTS – DTR
B12	VME bus interrupts	1 – 16 2 – 15 3 – 14 4 – 13 5 – 12 6 – 11 8 – 9	IRQ1 enabled IRQ2 enabled IRQ3 enabled IRQ4 enabled IRQ5 enabled IRQ6 enabled IRQ7 disabled VME PROM disabled
B13	User I/O, S/W readable	None	Not used
B14	Long time bus error enable	2 – 3	
B15	Threshold of the power voltage detector	1 – 4	4.65 to 4.70 volt threshold
B16	Serial interface MPCC2 RS232 control RS422/485 control	1 – 20 3 – 18 4 – 17 5 – 6 7 – 14 11 – 12 15 – 16	Bus request level 3

Table 5—4. MCP Jumper Configurations (Continued)			
JUMPER BLOCK	JUMPER BLOCK DESCRIPTION	JUMPERS INSTALLED	CONFIGURED JUMPER FUNCTION
B18	Abort to IRQ7	None	Not used
B19	Power standby for the SRAM 4.5V min.	None	Standby power disabled
B22	VSB enable/disable	1 — 2	VSB disabled

b. Referring to figure 5—3, identify SP7472300—XXX IC chip set and chip key placement.

c. Using standard commercial IC chip puller, carefully extract IC chip set (J21, J23, J25, and J27).

d. Place each chip in ESD approved conductive foam.

e. Package faulty MCP PWA as per procedure in section 2, paragraph 2—7

f. Place new MCP PWA on ESD approved work bench.

g. Referring to figure 5—3, re—insert SP7472300—XXX IC chip set. Ensure chip key placement is correct.

h Referring to figure 5—3 and table 5—4 verify/ ensure all MCP PWA jumper settings are correct.

i. Replace MCP PWA per procedure in paragraph 5—8.

5—10 Cooling Fan Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat—tipped screwdriver, loosen four captive screws and eight quick—disconnect screws securing top cover and remove top cover.

f. Remove air filter at rear of unit by sliding filter upward.

g. Disconnect/tag ac power plug from suspect fan.

h. Using a flat—tipped screwdriver, remove four each flat—head screws, flat washers, and lock nuts retaining faulty fan.

i. Remove faulty fan and protective cover.

j. Mount replacement fan and previously removed protective cover by replacing four each flat—head screws, flat washers, and lock washers previously removed in step (h).

k. Reconnect air filter ac power plug and air filter.

l. Replace top cover and using a flat—tipped screwdriver, tighten four top cover captive screws to maintenance panel and eight quick—disconnect screws to chassis.

m. Reconnect ac power cord to rear panel connector J101.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front—panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5–6 Operational Verification to verify MDP operability.

5–11 PS1 and PS2 Replacement

NOTE

Before replacing suspect faulty power supply, attempt to correct power supply fault by toggling unit power to reset power supply circuit breaker and then perform the adjustment procedures in paragraph 5–3.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

e. Applying pressure to bottom cover towards unit chassis, use a flat–tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

f. Carefully lower bottom panel to gain access to power supplies.

g. Tag all power lines connected to suspect power supply.

h. Disconnect power lines from power supply terminals using a flat–tipped screwdriver.

CAUTION

Secure power supply by applying pressure/firmly holding as mounting screws are removed. Failure to do so may result in damage to power supply due to slippage.

i. While applying pressure to power supply, use a No. 2 cross–tipped screwdriver to remove (four – PS2 or three – PS1) pan–head locking screws securing suspect power supply to bottom cover and store power supply in a secure area.

j. While firmly holding new power supply, use No. 2 cross–tipped screwdriver to replace (four – PS2 or three – PS1) pan–head locking screws removed in step (i) to secure power supply to bottom cover.

k. Reconnect power lines to their appropriate terminals using a flat–tipped screwdriver.

l. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

m. Reconnect ac power cord to rear panel connector J101.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front–panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5–6 Operational Verification to verify MDP operability.

5–12 Lamp Replacement

a. Grasp the lamp cover with the thumb and forefinger and remove it by unscrewing it from the lampholder assembly.

b. Grasp the lamp with the thumb and forefinger and remove it by pulling outward.

c. Reinsert replacement lamp; lamp is keyed so it will fit into lampholder only one way.

d. Replace lamp cover by screwing it back onto the lampholder; do not overtighten.

e Verify proper operation of replacement lamp by running the confidence BIT.

f. Perform paragraph 5—6 Operational Verification to verify MDP operability.

5—13 Lampholder Replacement

a. Preheat a soldering iron.

b. Set AC POWER ON/OFF switch to OFF.

c. Loosen the four captive screws holding the unit in the cabinet.

d. Slide the unit forward until the rail guide locks are set to the locked position.

e. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

f. Applying pressure to bottom cover towards unit chassis, use a flat—tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

g. Carefully lower bottom panel to gain access to suspect lampholder.

h. Remove protective heat shrink from lampholder connectors. Wrap may be removed by slipping it down the wire or by carefully cutting it off using a pair of snub—nosed wire cutters.

i. Tag lampholder wires connected to positive and negative leads.

j. Using preheated soldering iron, unsolder tagged wire connected to lampholder leads.

k. Using 1/2” open—end wrench, grasp mounting flange nut (on inside of front panel) holding lampholder to chassis. With free hand, grasp lampholder section on inside of front panel.

l. Unscrew flange nut and remove lampholder from chassis.

m. Replace new lampholder into front panel and screw flange nut finger tight onto chassis.

n. Using 1/2” open—end wrench, grasp mounting flange nut (on inside of front panel) holding lampholder to chassis. With free hand, grasp lampholder section on inside of front panel.

o. Tighten flange nut to ensure a firm mounting to chassis.

p. Place or ensure that an ample amount of shrink wrap is resident on each wire prior to soldering.

q. Using the preheated soldering iron, solder previously removed wires to respective positive and negative lampholder leads.

r. Shift the heat shrink so it covers the new soldered joint.

s. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

t. Reconnect ac power cord to rear panel connector J101.

u. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

v. Tighten four front—panel captive screws to the cabinet assembly.

w. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

x. Perform paragraph 5—6 Operational Verification to verify MDP operability.

5—14 Switches and Circuit Breaker Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

e. Applying pressure to bottom cover towards unit chassis, use a flat—tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

f. Carefully lower bottom panel to gain access to switches and circuit breaker.

g. Tag all wires connected to suspect switch or circuit breaker, after removing heatshrink that surrounds switch or circuit breaker with X—acto knife.

h. Using the appropriate flat—tipped or cross—tipped screwdriver, disconnect wire leads connected to suspect switch or circuit breaker.

i. Using 9/16” open—end wrench, grasp mounting flange nut (on outside of panel) holding suspect switch or circuit breaker to chassis. With free hand, grasp section on inside of panel.

j. Unscrew flange nut and remove from chassis.

k. Replace new switch or circuit breaker into panel and screw flange nut finger tight onto chassis.

l. Using 9/16” open—end wrench, grasp mounting flange nut (on outside of panel) holding switch or circuit breaker to chassis. With free hand, grasp section on inside of panel.

m. Tighten flange nut to ensure a firm mounting to chassis.

n. Place ample amount of heatshrink on switch.

o. Using appropriate flat—tipped or cross—tipped screwdriver, re—connect wire leads to new switch or circuit breaker.

p. Using a heat blower gun, form heatshrink over switch to adequately cover power leads.

q. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

r. Reconnect ac power cord to rear panel connector J101.

s. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

t. Tighten four front—panel captive screws to the cabinet assembly.

u. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

v. Perform paragraph 5—6 Operational Verification to verify MDP operability.

5—15 Preventive Maintenance

Preventive maintenance serves to keep the equipment in proper operating condition, to prevent breakdown, and to hold needless repair to a minimum. This information includes cleaning equipment required and instructions for preventive maintenance. As a general rule, the preventive maintenance measures detailed in the following paragraphs should be accomplished once a month or per site requirements. When the unit is

operated under severe contamination conditions (for example, dust or dirt) a shorter preventive maintenance interval is recommended. Turn off or disconnect the input power before performing the preventive maintenance procedures.

WARNING

Before attempting to perform inspection or preventive maintenance, ensure that power has been removed to prevent injury or DEATH from electric shock.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5—16 Inspection

Visual inspection of the unit should be performed once every 30 days or per site requirements. Visually inspect the unit to determine if the item is damaged or incomplete to the extent that it should be repaired or replaced. Perform the visual inspection procedures in table 5—5.

5—17 Preventive Maintenance Steps

Preventive maintenance consists of inspection, cleaning, and voltage checks. The unit should be cleaned every 30 days or per site requirements. Clean exterior surfaces using a clean lint—free cloth to remove dust or grease. Perform interior preventive maintenance as follows:

a. Using a vacuum cleaner, remove loose dust and dirt from card cage, PWAs, and interior surface.

b. Use a soft—bristle brush to remove dirt that adheres to the card cage, PWAs, and interior surfaces.

c. Remove air filter from behind 3—form frame, clean using a vacuum cleaner or reverse flushing with water, and replace air filter when dry.

d. Verify fan (3) rotation is free of restriction. Clean fan blades of dust accumulation.

e. Using a digital voltmeter, verify power supply voltages (via the maintenance panel test points) are within specification. Refer to paragraph 5—3 if adjustments are necessary.

Table 5—5. Inspection and Maintenance Criteria

ITEM	NOMENCLATURE	INSPECT FOR	REPAIR
1	Exterior	Dents, scratches, loose cable connectors, paint damage	Repair or replace
2	Interior	Dents, scratches, loose cable connectors, broken wires, evidence of burned or charred components, defective solder connections	Repair or replace

Section 6 — Parts List

6—1 Introduction

This section lists, describes, and illustrates a breakdown of items necessary to support the Modulator/Doppler Predictor. The purpose of the breakdown is to assist supply and maintenance personnel in identifying, requesting, and stockpiling MDP replacement parts.

6—2 List of Manufacturers

Table 6—2 contains the list of manufacturer commercial and government entity (CAGE) numbers/federal supply code for manufacturers (FSCM), names, and addresses for all items listed in the parts lists.

6—3 Maintenance Parts List

The maintenance parts lists (MPLs) (refer to table 6—1 for a list of MPLs, tables 6—3 through 6—6) provide a description of each major assembly, subassembly, and attaching part listed, keyed to the applicable figure (e.g., figure 6—2, index 4 is identified in the first column of the corresponding MPL as 6—2—4). Other information in the MPLs include item reference designator, item nomenclature/description, manufacturer's code (CAGE/FSCM), item part number, and number of units per assembly. These items are all described in the following paragraphs.

6—4 Reference Designator Column

The reference designator allows for an indexed item designation reference to the top assembly.

6—5 Figure and Index Number Column

This column lists the applicable index numbers called out on the associated figure.

6—6 Description Column

This column contains the nomenclature and description of each assembly, subassembly, or attaching part. Subassemblies within an assembly are indented under that assembly with individual index numbers assigned to them. Attaching parts hardware is indented under the item it attaches, and the description is followed by the attaching part annotation "(AP)."

6—7 CAGE/FSCM Column

This column provides the parts manufacturers' CAGE/FSCM codes. These codes relate to the manufacturers listed in table 6—2 and are in accordance with Federal Supply Codes for Manufacturers Cataloging books H4—1, H4—2, and H4—3.

6—8 Part Number Column

This column contains the manufacturer's part number for the indexed part in the associated figure. A number sign (#) following the part number indicates that the item is either government—furnished equipment (GFE), contractor—furnished equipment (CFE), or attachment hardware covered in other manuals.

6—9 Quantity Column

This column indicates the quantity required for an assembly, subassembly, or piece part. If quantities are indefinite (i.e., adhesive, locktite, etc.), an "AR" is placed in this column to indicate "as required." If the quantity of the item has been called out in a previous figure or if the item must be removed to gain access to a spared item, a "REF" is placed in this column to indicate "reference".

6—10 Illustrations

Figures 6—1 through 6—4 (refer to table 6—1 for a list of parts illustrations) are illustrated parts breakdowns (IPBs) showing the major assemblies, subassemblies, and attaching parts associated with the MDP. Individual items in each figure are identified with an index number and keyed to the corresponding MPL, which normally faces and immediately follows the figure.

Table 6—1. List of Parts Lists and Figures

TABLE NO.	FIGURE NO.	TITLE	PAGE NO.
	6—1	Modulator/Doppler Predictor (Top View)	6—4
6—3		Parts List, Modulator/Doppler Predictor (Top View)	6—5
	6—2	Modulator/Doppler Predictor (Front View)	6—6
6—4		Parts List, Modulator/Doppler Predictor (Front View)	6—7
	6—3	Modulator/Doppler Predictor (Side View)	6—8
6—5		Parts List, Modulator/Doppler Predictor (Side View)	6—9
	6—4	Modulator/Doppler Predictor (Rear View)	6—10
6—6		Parts List, Modulator/Doppler Predictor (Rear View)	6—11

Table 6—2. Index to Manufacturers CAGE/FSCM Numbers

CAGE/ FSCM	MANUFACTURER	ADDRESS
03102	Supreme Supply Co.	734 E. Hyde Park Blvd. P.O. Box 922 Inglewood, CA 90302—2508
05236	Jonathan Mfg. Co.	Fullerton, CA
07421	Interstate Electronics Corp.	1001 E. Ball Road P.O. Box 3117 Anaheim, CA 92803
08742	Emerson Electric Co.	ACDC Electrics Div. 401 Jones Rd. Oceanside, CA 92054—1216
09353	C and K Components Inc.	15 Riverdale Ave. Newton, MA 02158—1057
25140	Globe Motors	2275 Stanley Ave. Dayton, Ohio 45404
27193	Eaton Corp.	Aerospace/Commercial Controls Div. Milwaukee, WI
72619	Dialight Corp.	Brooklyn Div. 203 Harrison Pl. Brooklyn, New York 11237—1587
80103	VEECO Instruments Inc.	Lambda Electronics Div. 515 Broad Hollow Rd. Melville, New York 11747—3703
80205	National Aerospace Standards Committee Aerospace Industries Association of America, Washington, DC. Sources of supply for all of the National Aerospace Standards have been identified and compiled into a reference book published by the National Standards Association. This book is available through Federal Supply Schedule 76, Part I.	
81349	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3—M.	
8Z410	Ledtronics Inc.	Harbor City, CA
96906	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3—M.	
NMB	NMB Technologies Inc.	Motor Division Chatsworth, CA
WSC	White Sands Complex	Box 9000 Las Cruces, NM

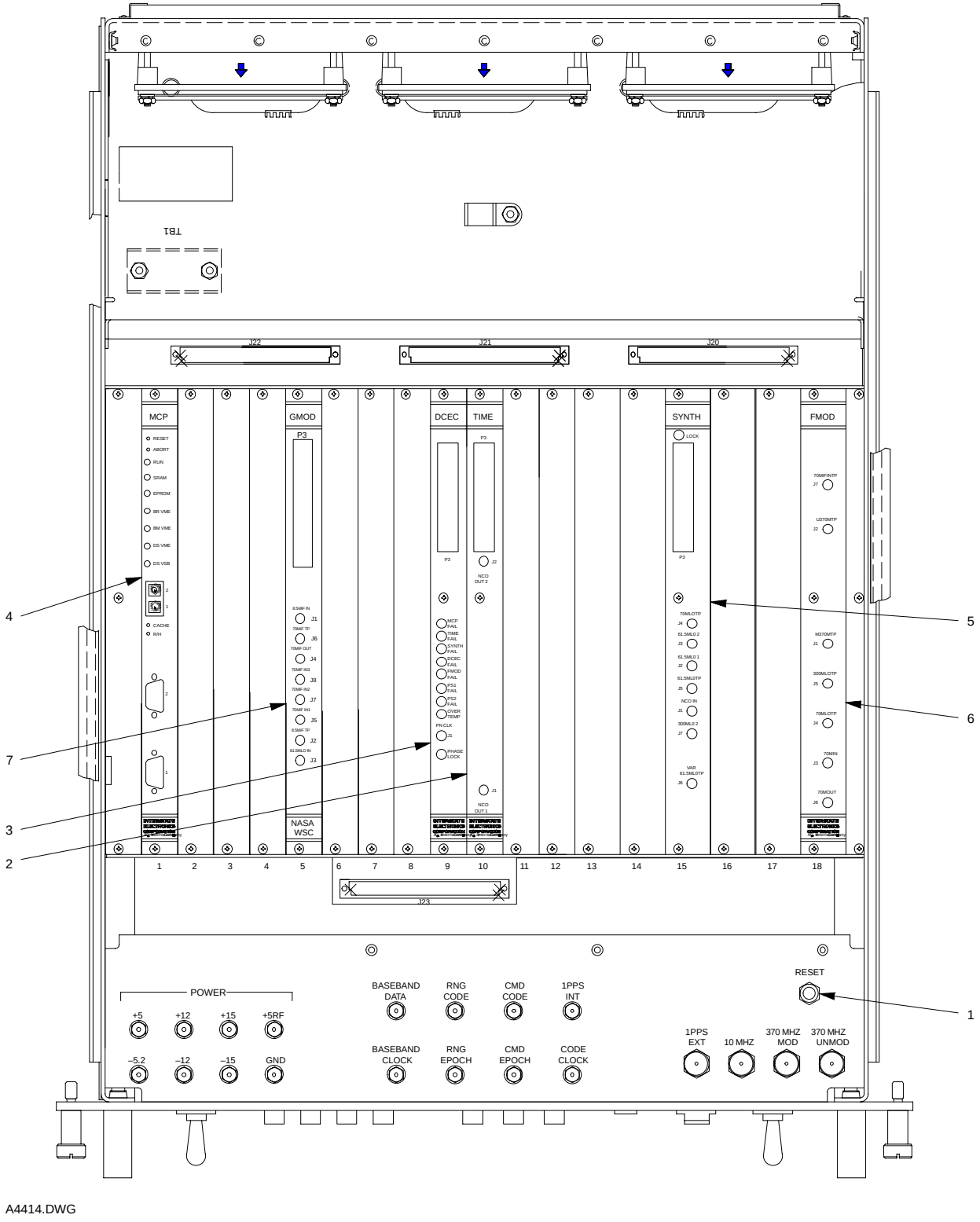

Figure 6—1. Modulator/Doppler Predictor (Top View)

Table 6—3. Parts List, Modulator/Doppler Predictor (Top View)

REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—1	Modulator/Doppler Predictor (Top View)	07421	7472300	REF
1A6SW4	6—1—1	. Switch, Push . . Cap, Nylon (AP)	09353 09353	8121ZE 7527—2	1 1
1A4A10	6—1—2	. Timing Generator PWA	07421	7473000—502	1
1A4A9	6—1—3	. Data Conditioning and Encoding PWA	07421	7473800—501	1
1A4A1	6—1—4	. Modem Control Processor PWA . . Firmware Chip Set (J21, J23, J25, and J29) (AP)	07421 07421	7473600 SP7472300—XXX (*)	1 1
1A4A15	6—1—5	. Synthesizer PWA	07421	7474600—500	1
1A4A18	6—1—6	. Forward Modulator PWA	07421	7474800	1
1A4A5	6—1—7	GN Modulator PWA (SSA configuration only)	WSC	1547558	1

Note: * (XXX) represents the current firmware version. Refer to figure 5—3 for chip location/placement.

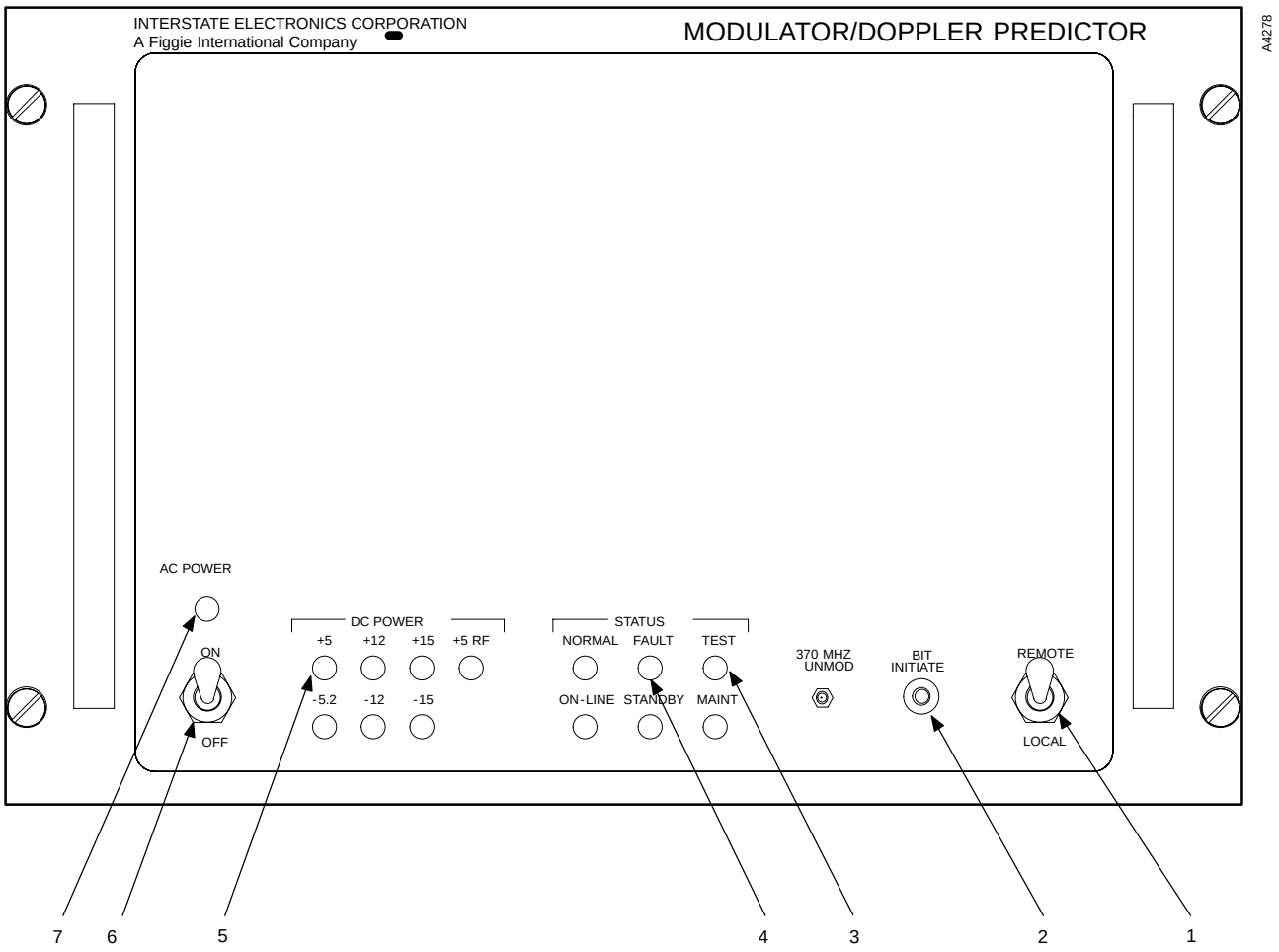

Figure 6—2. Modulator/Doppler Predictor (Front View)

Table 6—4. Parts List, Modulator/Doppler Predictor (Front View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—2	Modulator/Doppler Predictor (Front View)	07421	7472300	REF
1A7SW2	6—2—1	. Switch, Toggle	96906	MS24658—23F	1
1A7SW3	6—2—2	. Switch, Pushbutton	27193	W403PGR	1
1A7DS8	6—2—3	. Lamp, Cartridge . . Lampholder	72619 8Z410	507—4957—3733—500 DH0—30Y—D86BWC	1 1
1A7DS7	6—2—4	. Lamp, Cartridge . . Lampholder	72619 8Z410	507—4757—3731—500 DH0—30Y—D86BWC	1 1
1A7DS2—DS6,DS9—DS14	6—2—5	. Lamp, Cartridge . . Lampholder	72619 8Z410	507—4857—3732—500 DH0—30Y—D86BWC	1 1
1A7SW1	6—2—6	. Switch	81349	MS24659—22F	1
1A7DS1	6—2—7	. Lamp (LED), Cartridge	8Z410	CF296CWPG6—120VAC—R	1

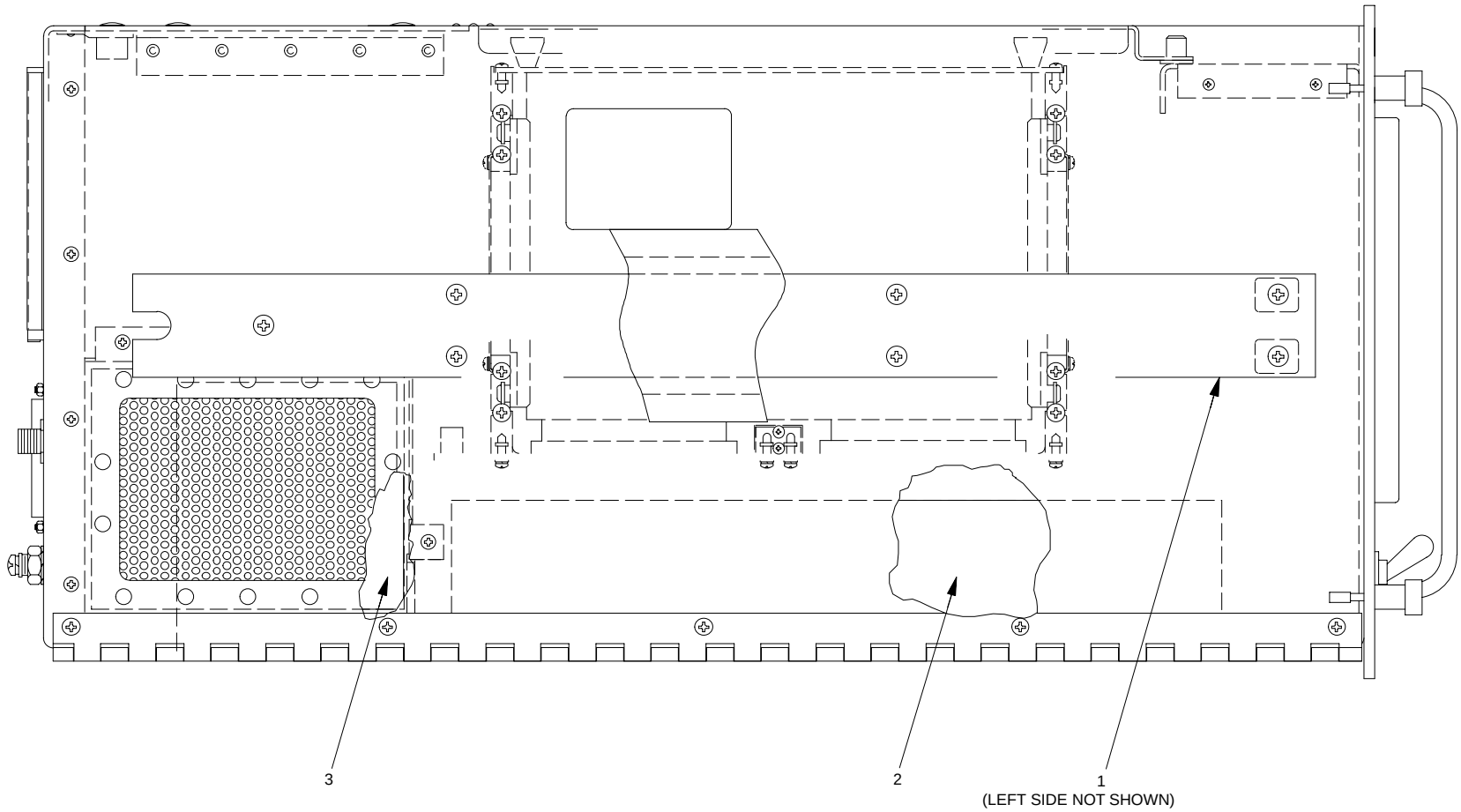

Figure 6—3. Modulator/Doppler Predictor (Side View)

Table 6—5. Parts List, Modulator/Doppler Predictor (Side View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—3	Modulator/Doppler Predictor (Side View)	07421	7472300	REF
	6—3—1 (Not Shown)	. Slide, Section (Left)	05236	1505772B—L	1
		. . Screw, Cres FLH100 10—32X5/8 (AP)	96906	MS24693—C273	7
	6—3—1	. Slide, Section (Right)	05236	1505772B—R	1
		. . Screw, Cres FLH100 10—32X5/8 (AP)	96906	MS24693—C273	7
1A3	6—3—2	. Power Supply No. 2	08742	RMV223B—2330—0450	1
		. . Screw, PNH—LKG (AP)	80205	NAS1635—08LL8	4
		. . Washer (AP)	80205	MS15795—807	4
1A2	6—3—3	. Power Supply No. 1	80103	LFQ—27—1	1
		. . Screw, PNH—LKG (AP)	80205	NAS1635—08LL8	3
		. . Washer (AP)	80205	MS15795—807	3

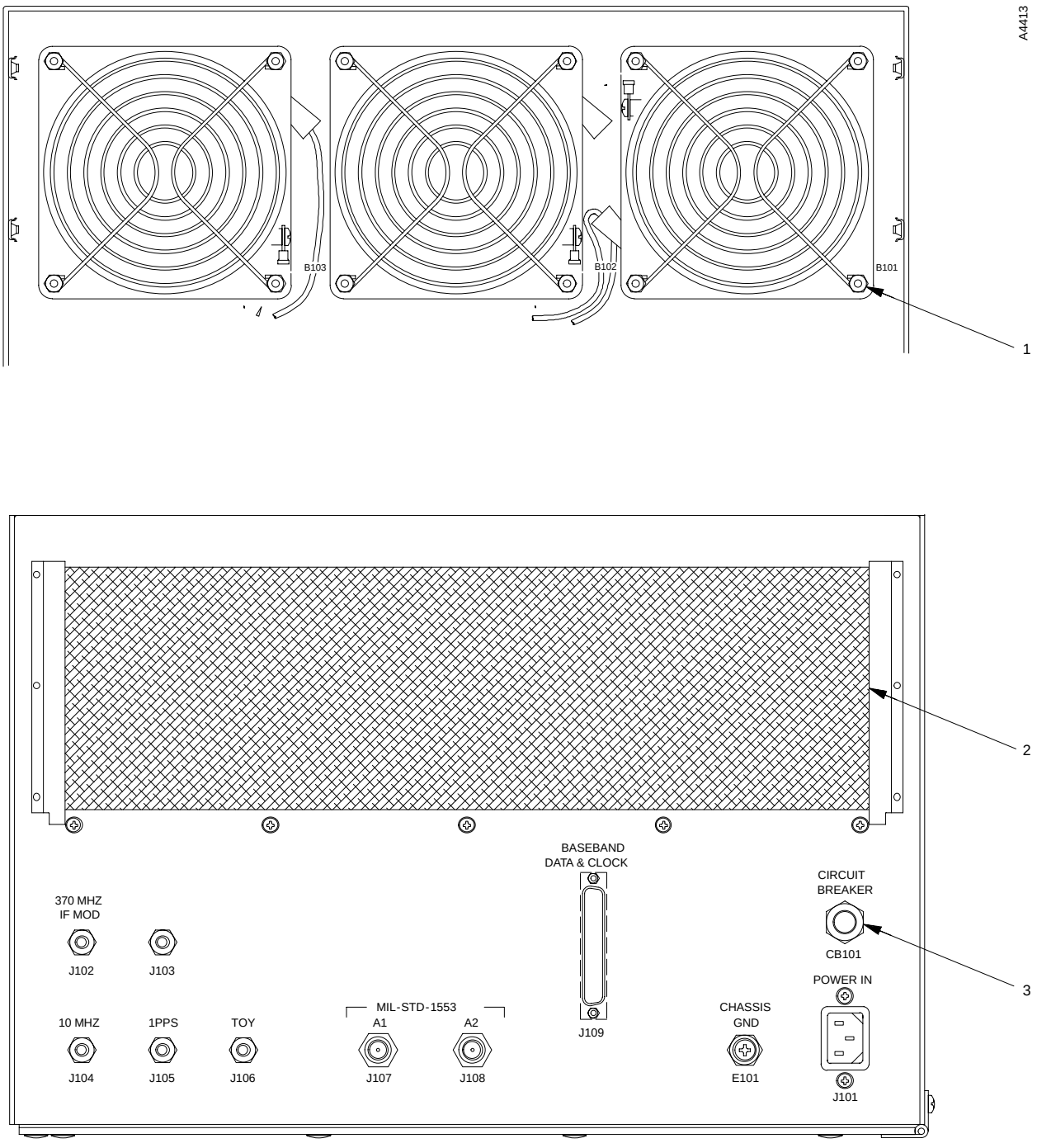

Figure 6—4. Modulator/Doppler Predictor (Rear View)

Table 6—6. Parts List, Modulator/Doppler Predictor (Rear View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6—4	Modulator/Doppler Predictor (Rear View)	07421	7472300	REF
1A1B101—B103	6—4—1	. Fan, Tubeaxial	25140	A47—B15A—15T3—000	3
		. . Grille, Metal (AP)	NMB	055015	4
		. . Screw, FLH 100 6—32X7/16 (AP)	96906	MS24693—C40	4
		. . Washer (AP)	96906	MS15795—805	4
		. . Nut (AP)	96906	MS21045C06	4
	6—4—2	. Filter, Air Cond	03102	3994—A	1
1A1CB101	6—4—3	. Circuit Breaker	81349	MS25244—10	1

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Section 7 — Drawings

7—1 Introduction

This section refers to drawings necessary for maintenance technicians to understand the makeup and function of the power, control, and signal inputs/outputs to and from the MDP major components and subcomponents. These drawings allow the technicians to trace the path of each input/output, make continuity checks, perform general and specific trouble analysis of inoperative or malfunctioning MDP functions, and locate components within the MDP. Refer to table 7—1 for a list of drawings necessary for Level 1 maintenance.

Table 7—1. List of Drawings

FIGURE NUMBER	TITLE	DRAWING NUMBER
	Modulator/Doppler Predictor Schematic Logic Diagram	EL7472301

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Glossary

The following defines the abbreviations, acronyms, and mnemonics used in this manual.

ADPE	Automated data processing equipment
AGC	Automatic gain control
ALC	Automatic level control
ASIC	Application—specific integrated circuit
AP	Attaching part
AR	As required
A/D	Analog to digital
BB	Baseband
BCD	Binary—coded digital
BER	Bit error rate
BERT	Bit error rate tester
BIM	Bus interrupter module
BIT	Built—in test
BITE	BIT equipment
BPF	Band—pass filter
BPSK	Binary PSK
CAGE	Commercial and government entity
CC	Common carrier
COTS	Commercial off—the—shelf
CPU	Central processing unit
CTFS	Common time and frequency system
CW	Continuous wave
C/No	Carrier—to—noise—density ratio
DAC	Digital—to—analog converter
dB	Decibel
dBm	Decibel unit of power level with reference to a power of one milliwatt
DCEC	Data conditioning and encoding PWA
DoD	Department of Defense
DPRAM	Dual—ported RAM
DSP	Digital signal processor
D/A	Digital to analog
Eb/No	Bit energy—to—noise ratio
ECL	Emitter—coupled logic
EIRP	Effective isotropic radiated power
EMI	Electromagnetic interference
EPROM	Electrically programmable ROM
ESD	Electrostatic discharge
Exec	Executive Program
FDU	Functional design unit
FFT	Fast Fourier Transform
FIR	Finite impulse response
FMOD	Forward modulator PWA
FPCP	Floating—point coprocessor
FSCM	Federal supply code for manufacturers
GN	Ground network
GT	Ground terminal
HDR	High data rate
HMD	Hardware maintenance depot
HWCI	Hardware configuration item
I	Inphase
IC	Integrated Circuit
IEC	Interstate Electronics Corporation
IF	Intermediate frequency
IPB	Illustrated parts breakdown
IR	Integrated receiver
IRIG	Inter—range instrumentation group
ISR	Interrupt service routine
I/D	Integrate/dump
I/O	Input/output
kbps	kilobits per second
KSA	K—band single access
KSAF	KSA forward service
KSH	K—band shuttle
KSHF	K—band shuttle forward service
LBI	Local bus interface
LDR	Low data rate
LMT	Line maintenance technician

LO	Local oscillator
LPF	Lowpass filter
LRU	Line replaceable unit
LSB	Least significant bit
MA	Multiple access
MAF	MA forward service
Mbps	Megabits per second
MCP	Modem control processor PWA
MDP	Modulator/Doppler Predictor
MHz	Megahertz
Mmax	Maximum—time—to—repair
MPCC	Multiprotocol communications controller
MPL	Maintenance parts list
MSB	Most significant bit
MTG	Maintenance test group
MTTR	Mean—time—to—repair
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NASCOM	NASA communications network
NCO	Numerically controlled oscillator
NGT	NASA ground terminal
NRZ—L	Nonreturn to zero—level
NRZ—M	Nonreturn to zero—mark
NRZ—S	Nonreturn to zero—space
O&M	Operation and maintenance
PE	Probability of error
PIT	Programmable interval timer
PI/T	Parallel interface and timer
PLL	Phased—lock loop
PMMS	Performance measuring and monitoring system
PN	Pseudo—random noise
PS	Power supply
PSK	Phase—shift keying
PTE	PMMS test equipment
p—p	Peak—to—peak
QPSK	Quadrature PSK
RAM	Random access memory
RF	Radio frequency
ROM	Read—only memory
RTA	Remote terminal address
RTC	Real—time clock
R/H	Run/halt
R/R	Removal/replacement
SN	Space network
SQPSK	Staggered quadrature PSK
SRAM	Static RAM
SSA	S—band single access
SSAF	SSA forward service
SSH	S—band shuttle
SSHF	S—band shuttle forward service
STDN	Spaceflight tracking and data network
STGT	Second TDRSS Ground Terminal
	Tracking and Data Relay Satellite System
SYNTH	Synthesizer PWA
TB	Terminal board
TDRSS	Tracking and data relay satellite system
TIME	Timing Generator PWA
TN	TDRSS network
TOCC2	TDRS operations control center No. 2
TOY	Time—of—year
TS	Tri—state
TTL	Transistor—transistor logic
UQPSK	Unbalanced QPSK
USAT	User satellite
USS	User services subsystem
Vac	Voltage alternating current
VCO	Voltage controlled oscillator
VCXO	Voltage controlled crystal oscillator
Vdc	Voltage direct current
VME	Versa—Module Europa
VRTX	Versatile Real Time Executive